Allegro® MicroSystems, Inc.

A4988

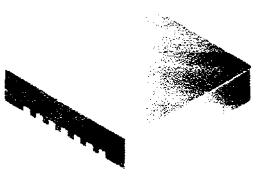
DMOS Microstepping Driver with Translator and Overcurrent Protection

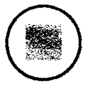
Features and Benefits

- Low $R_{DS(ON)}$ outputs
- Automatic current decay mode detection/selection
- Mixed and Slow current decay modes
- Synchronous rectification for low power dissipation
- Internal UVLO
- Crossover-current protection
- 3.3 and 5 V compatible logic supply
- Thermal shutdown circuitry
- Short-to-ground protection
- Shorted load protection
- Five selectable step modes: full, $^1/_2$, $^1/_4$, $^1/_8$, and $^1/_{16}$

Package:

28-contact QFN
with exposed thermal pad
5 mm × 5 mm × 0.90 mm
(ET package)





Approximate size

Description

The A4988 is a complete microstepping motor driver with built-in translator for easy operation. It is designed to operate bipolar stepper motors in full-, half-, quarter-, eighth-, and sixteenth-step modes, with an output drive capacity of up to 35 V and ±2 A. The A4988 includes a fixed off-time current regulator which has the ability to operate in Slow or Mixed decay modes.

The translator is the key to the easy implementation of the A4988. Simply inputting one pulse on the STEP input drives the motor one microstep. There are no phase sequence tables, high frequency control lines, or complex interfaces to program. The A4988 interface is an ideal fit for applications where a complex microprocessor is unavailable or is overburdened.

During stepping operation, the chopping control in the A4988 automatically selects the current decay mode, Slow or Mixed. In Mixed decay mode, the device is set initially to a fast decay for a proportion of the fixed off-time, then to a slow decay for the remainder of the off-time. Mixed decay current control results in reduced audible motor noise, increased step accuracy, and reduced power dissipation.

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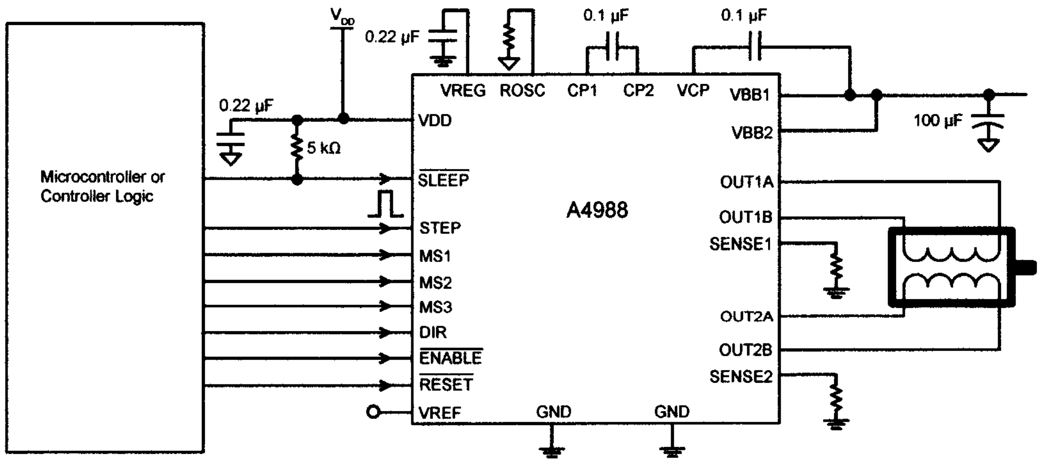
Typical Application Diagram



4988-DS, Rev. 1

scription (continued)

ernal synchronous rectification control circuitry is provided improve power dissipation during PWM operation. Internal cuit protection includes: thermal shutdown with hysteresis, dervoltage lockout (UVLO), and crossover-current protection. ecial power-on sequencing is not required.

The A4988 is supplied in a surface mount QFN package (ES), 5 mm × 5 mm, with a nominal overall package height of 0.90 mm and an exposed pad for enhanced thermal dissipation. It is lead (Pb) free (suffix –T), with 100% matte tin plated leadframes.

election Guide

Part Number	Package	Packing
4988SETTR-T	28-contact QFN with exposed thermal pad	1500 pieces per 7-in. reel

bsolute Maximum Ratings

Characteristic	Symbol	Notes	Rating	Units
oad Supply Voltage	V_{BB}		35	V
utput Current	I_{OUT}		±2	A
ogic Input Voltage	V_{IN}		–0.3 to 5.5	V
ogic Supply Voltage	V_{DD}		–0.3 to 5.5	V
BBx to OUTx			35	V
ense Voltage	V_{SENSE}		0.5	V
eference Voltage	V_{REF}		5.5	V
perating Ambient Temperature	T_A	Range S	–20 to 85	°C
laximum Junction	$T_J(max)$		150	°C
torage Temperature	T_{stg}		–55 to 150	°C

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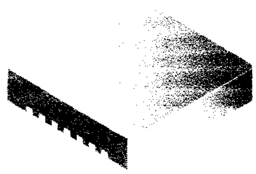

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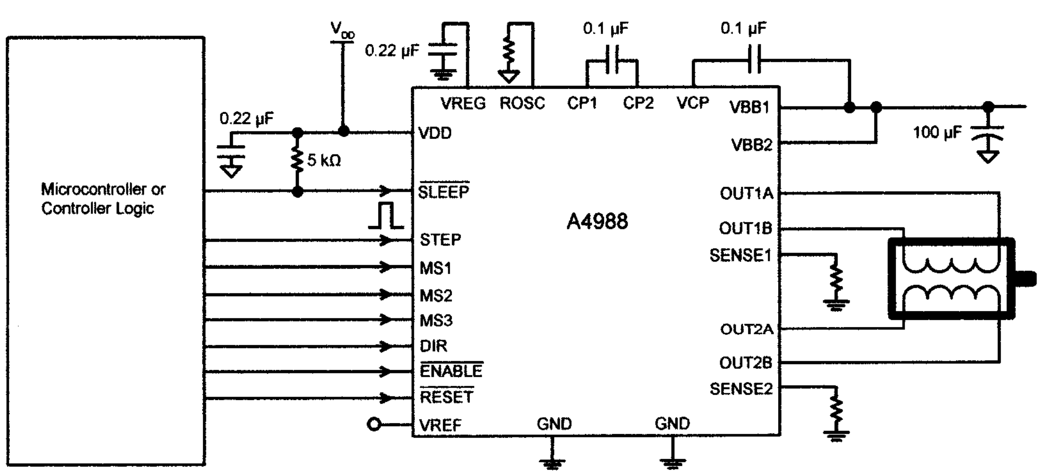
Typical Application Diagram



scription (continued)

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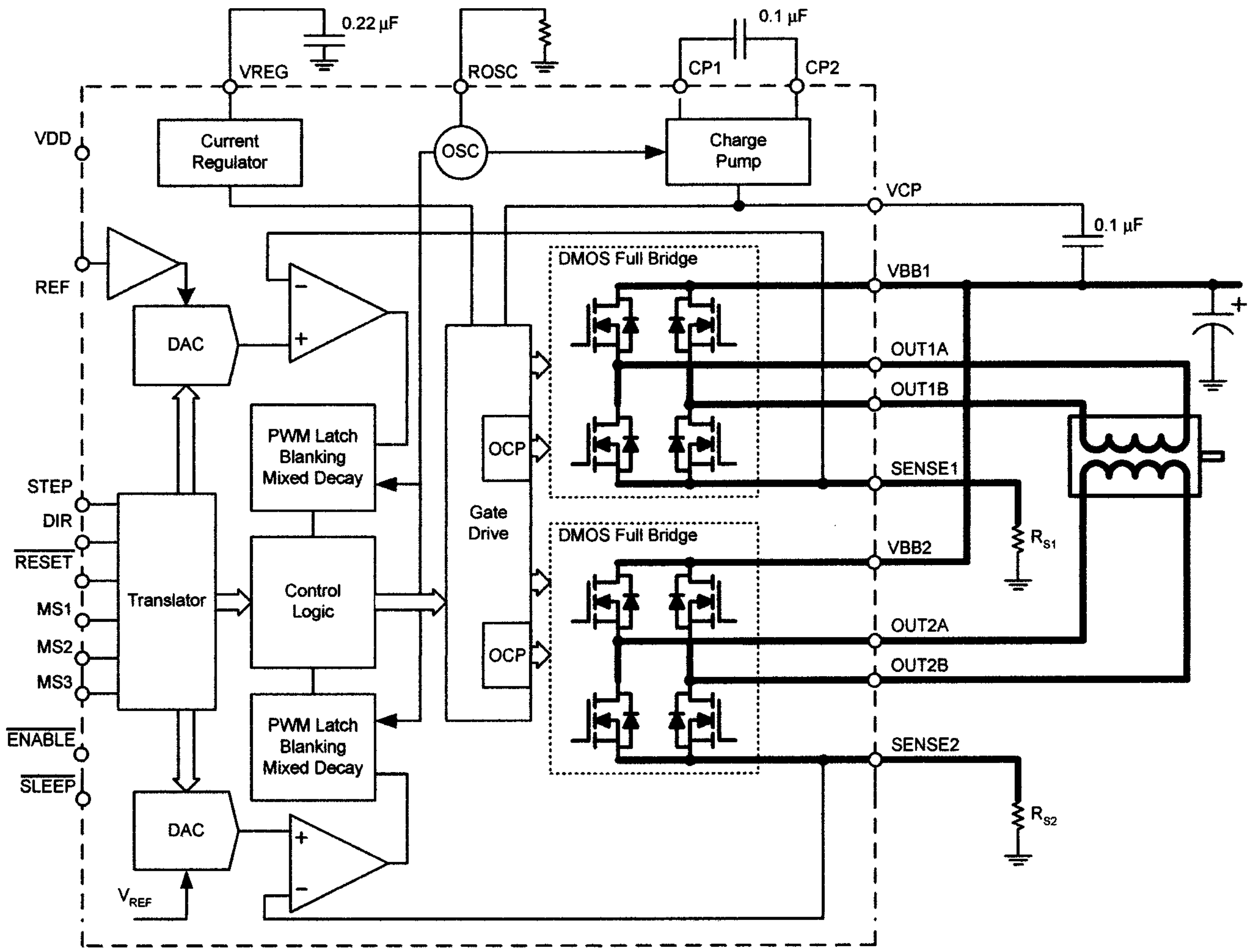
ogic Supply Voltage	V_{DD}		–0.3 to 5.5	V
BBx to OUTx			35	V
ense Voltage	V_{SENSE}		0.5	V
eference Voltage	V_{REF}		5.5	V
perating Ambient Temperature	T_A	Range S	–20 to 85	°C
aximum Junction	T_J(max)		150	°C
torage Temperature	T_{stg}		–55 to 150	°C

Functional Block Diagram



ECTRICAL CHARACTERISTICS[1] at T_A = 25°C, V_{BB} = 35 V (unless otherwise noted)

Characteristics	Symbol	Test Conditions	Min.	Typ.[2]	Max.	Units
tput Drivers						
ad Supply Voltage Range	V_{BB}	Operating	8	–	35	V
gic Supply Voltage Range	V_{DD}	Operating	3.0	–	5.5	V
tput On Resistance	R_{DSON}	Source Driver, I_{OUT} = –1.5 A	–	320	430	mΩ
		Sink Driver, I_{OUT} = 1.5 A	–	320	430	mΩ
dy Diode Forward Voltage	V_F	Source Diode, I_F = –1.5 A	–	–	1.2	V
		Sink Diode, I_F = 1.5 A	–	–	1.2	V
tor Supply Current	I_{BB}	f_{PWM} < 50 kHz	–	–	4	mA
		Operating, outputs disabled	–	–	2	mA
gic Supply Current	I_{DD}	f_{PWM} < 50 kHz	–	–	8	mA
		Outputs off	–	–	5	mA
ntrol Logic						
gic Input Voltage	$V_{IN(1)}$		V_{DD}×0.7	–	–	V
	$V_{IN(0)}$		–	–	V_{DD}×0.3	V
gic Input Current	$I_{IN(1)}$	V_{IN} = V_{DD}×0.7	–20	<1.0	20	μA
	$I_{IN(0)}$	V_{IN} = V_{DD}×0.3	–20	<1.0	20	μA
crostep Select	R_{MS1}	MS1 pin	–	100	–	kΩ
	R_{MS2}	MS2 pin	–	50	–	kΩ
	R_{MS3}	MS3 pin	–	100	–	kΩ
gic Input Hysteresis	$V_{HYS(IN)}$	As a % of V_{DD}	5	11	19	%
ank Time	t_{BLANK}		0.7	1	1.3	μs
xed Off-Time	t_{OFF}	OSC = VDD or GND	20	30	40	μs
		R_{OSC} = 25 kΩ	23	30	37	μs
eference Input Voltage Range	V_{REF}		0	–	4	V
eference Input Current	I_{REF}		–3	0	3	μA
rrent Trip-Level Error[3]	err_I	V_{REF} = 2 V, $\%I_{TripMAX}$ = 38.27%	–	–	±15	%
		V_{REF} = 2 V, $\%I_{TripMAX}$ = 70.71%	–	–	±5	%
		V_{REF} = 2 V, $\%I_{TripMAX}$ = 100.00%	–	–	±5	%
ossover Dead Time	t_{DT}		100	475	800	ns
otection						
vercurrent Protection Threshold	I_{OCPST}		2.1	–	–	A
ermal Shutdown Temperature	T_{TSD}		–	165	–	°C
ermal Shutdown Hysteresis	T_{TSDHYS}		–	15	–	°C
D Undervoltage Lockout	V_{DDUVLO}	V_{DD} rising	2.7	2.8	2.9	V
D Undervoltage Hysteresis	$V_{DDUVLOHYS}$		–	90	–	mV

r input and output current specifications, negative current is defined as coming out of (sourcing) the specified device pin.

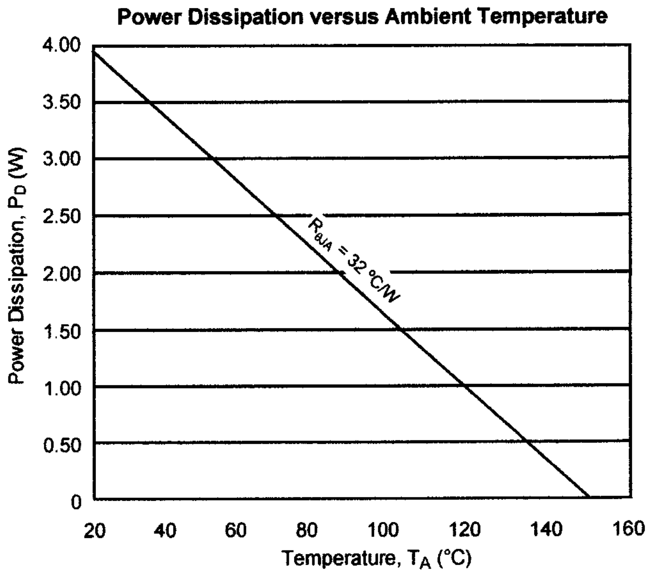
pical data are for initial design estimations only, and assume optimum manufacturing and application conditions. Performance may vary for individual ts, within the specified maximum and minimum limits.

$_{ERR}$ = [(V_{REF}/8) – V_{SENSE}] / (V_{REF}/8).

THERMAL CHARACTERISTICS

Characteristic	Symbol	Test Conditions*	Value	Units
Package Thermal Resistance	$R_{\theta JA}$	Four-layer PCB, based on JEDEC standard	32	°C/W

*Additional thermal information available on Allegro Web site.



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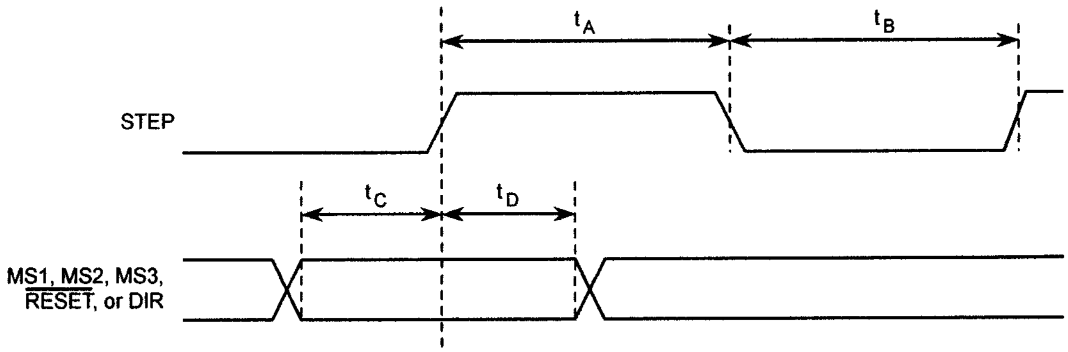

Time Duration	Symbol	Typ.	Unit
STEP minimum, HIGH pulse width	t_A	1	μs
STEP minimum, LOW pulse width	t_B	1	μs
Setup time, input change to STEP	t_C	200	ns
Hold time, input change to STEP	t_D	200	ns

Figure 1. Logic Interface Timing Diagram

Table 1. Microstepping Resolution Truth Table

MS1	MS2	MS3	Microstep Resolution	Excitation Mode
L	L	L	Full Step	2 Phase
H	L	L	Half Step	1-2 Phase
L	H	L	Quarter Step	W1-2 Phase
H	H	L	Eighth Step	2W1-2 Phase
H	H	H	Sixteenth Step	4W1-2 Phase

Functional Description

vice Operation. The A4988 is a complete microstepping tor driver with a built-in translator for easy operation with nimal control lines. It is designed to operate bipolar stepper tors in full-, half-, quarter-, eighth, and sixteenth-step modes. e currents in each of the two output full-bridges and all of the channel DMOS FETs are regulated with fixed off-time PWM lse width modulated) control circuitry. At each step, the current each full-bridge is set by the value of its external current-sense istor (R_{S1} and R_{S2}), a reference voltage (V_{REF}), and the output tage of its DAC (which in turn is controlled by the output of translator).

power-on or reset, the translator sets the DACs and the phase rent polarity to the initial Home state (shown in figures 8 ough 12), and the current regulator to Mixed Decay Mode for h phases. When a step command signal occurs on the STEP ut, the translator automatically sequences the DACs to the t level and current polarity. (See table 2 for the current-level quence.) The microstep resolution is set by the combined effect the MSx inputs, as shown in table 1.

ien stepping, if the new output levels of the DACs are lower n their previous output levels, then the decay mode for the ive full-bridge is set to Mixed. If the new output levels of the Cs are higher than or equal to their previous levels, then the ay mode for the active full-bridge is set to Slow. This auto- tic current decay selection improves microstepping perfor- nce by reducing the distortion of the current waveform that ults from the back EMF of the motor.

crostep Select (MSx). The microstep resolution is set by voltage on logic inputs MSx, as shown in table 1. The MS1 and 3 pins have a 100 kΩ pull-down resistance, and the MS2 pin a 50 kΩ pull-down resistance. When changing the step mode change does not take effect until the next STEP rising edge.

he step mode is changed without a translator reset, and abso- e position must be maintained, it is important to change the p mode at a step position that is common to both step modes in ler to avoid missing steps. When the device is powered down, reset due to TSD or an over current event the translator is set to home position which is by default common to all step modes.

Mixed Decay Operation. The bridge operates in Mixed decay mode, at power-on and reset, and during normal running according to the ROSC configuration and the step sequence, as shown in figures 8 through 12. During Mixed decay, when the trip point is reached, the A4988 initially goes into a fast decay mode for 31.25% of the off-time, t_{OFF}. After that, it switches to Slow decay mode for the remainder of t_{OFF}. A timing diagram for this feature appears on the next page.

Typically, mixed decay is only necessary when the current in the winding is going from a higher value to a lower value as determined by the state of the translator. For most loads automatically-selected mixed decay is convenient because it minimizes ripple when the current is rising and prevents missed steps when the current is falling. For some applications where microstepping at very low speeds is necessary, the lack of back EMF in the winding causes the current to increase in the load quickly, resulting in missed steps. This is shown in figure 2. By pulling the ROSC pin to ground, mixed decay is set to be active 100% of the time, for both rising and falling currents, and prevents missed steps as shown in figure 3. If this is not an issue, it is recommended that automatically-selected mixed decay be used, because it will produce reduced ripple currents. Refer to the Fixed Off-Time section for details.

Low Current Microstepping. Intended for applications where the minimum on-time prevents the output current from regulating to the programmed current level at low current steps. To prevent this, the device can be set to operate in Mixed decay mode on both rising and falling portions of the current waveform. This feature is implemented by shorting the ROSC pin to ground. In this state, the off-time is internally set to 30 μs.

Reset Input ($\overline{\text{RESET}}$). The $\overline{\text{RESET}}$ input sets the translator to a predefined Home state (shown in figures 8 through 12), and turns off all of the FET outputs. All STEP inputs are ignored until the $\overline{\text{RESET}}$ input is set to high.

Step Input (STEP). A low-to-high transition on the STEP input sequences the translator and advances the motor one increment. The translator controls the input to the DACs and the direc-

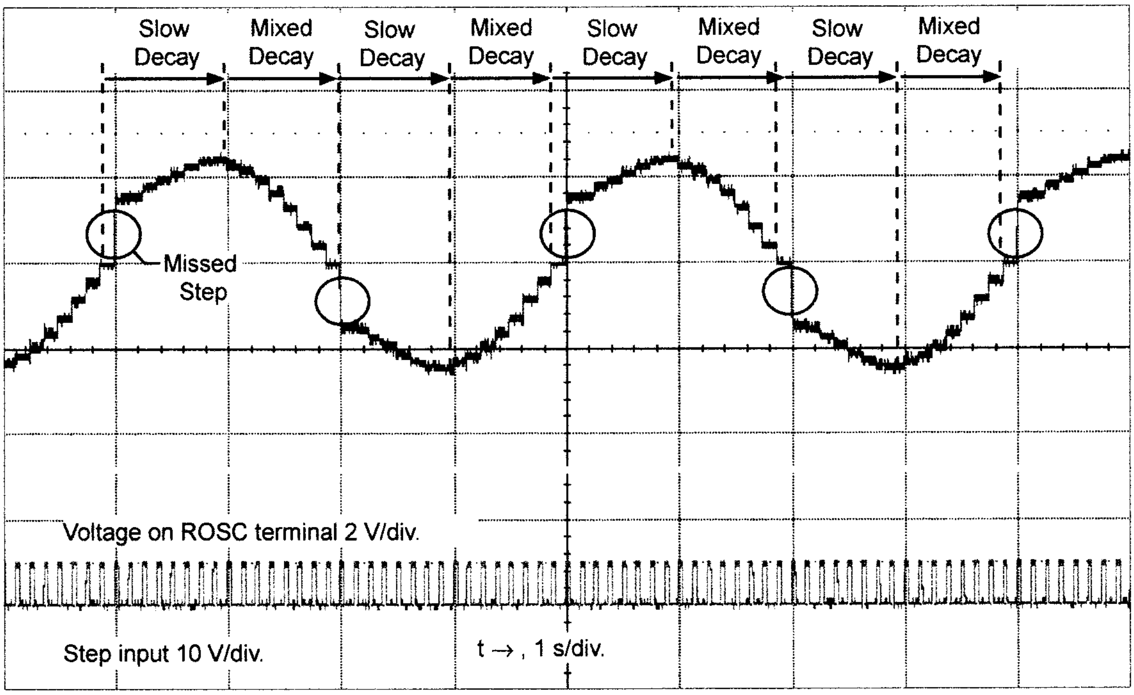

Figure 2. Missed steps in low-speed microstepping

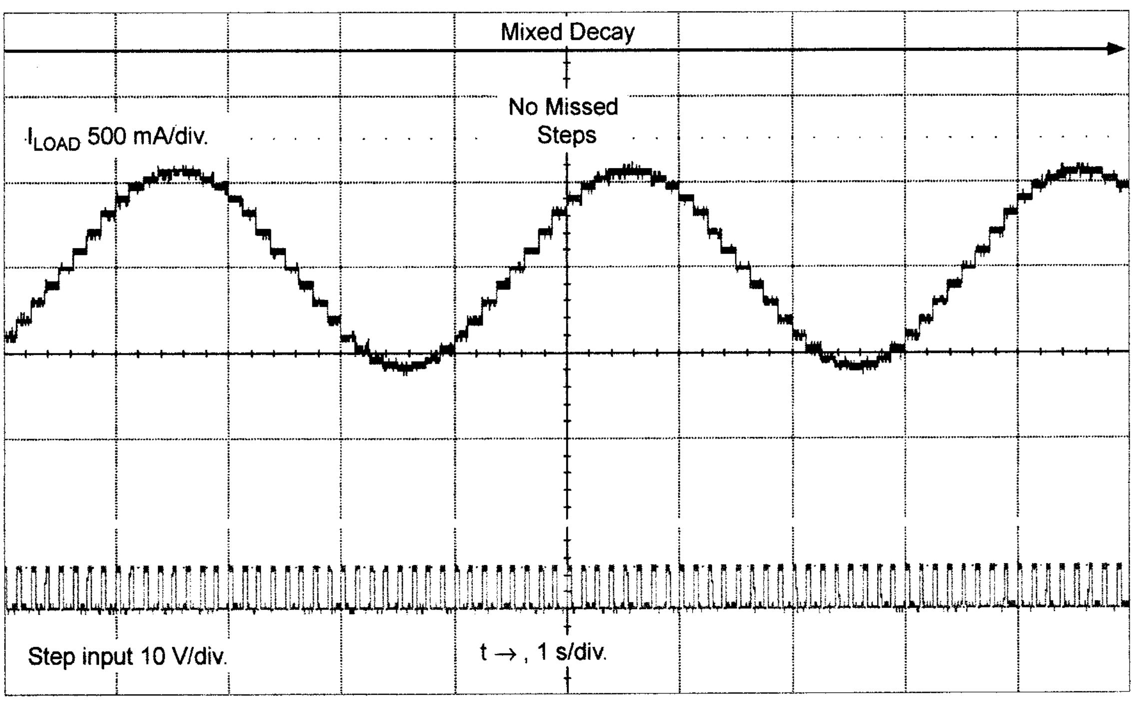

Figure 3. Continuous stepping using automatically-selected mixed stepping (ROSC pin grounded)

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n of current flow in each winding. The size of the increment is termined by the combined state of the MSx inputs.

rection Input (DIR). This determines the direction of rotan of the motor. Changes to this input do not take effect until the xt STEP rising edge.

ternal PWM Current Control. Each full-bridge is conlled by a fixed off-time PWM current control circuit that limits load current to a desired value, I_{TRIP}. Initially, a diagonal pair source and sink FET outputs are enabled and current flows rough the motor winding and the current sense resistor, R_{Sx}. hen the voltage across R_{Sx} equals the DAC output voltage, the rrent sense comparator resets the PWM latch. The latch then rns off the appropriate source driver and initiates a fixed off ne decay mode

e maximum value of current limiting is set by the selection of $_x$ and the voltage at the VREF pin. The transconductance funcn is approximated by the maximum value of current limiting, $_{ipMAX}$ (A), which is set by

$$I_{TripMAX} = V_{REF} / (8 \times R_S)$$

ere R_S is the resistance of the sense resistor (Ω) and V_{REF} is input voltage on the REF pin (V).

e DAC output reduces the V_{REF} output to the current sense mparator in precise steps, such that

$$I_{trip} = (\%I_{TripMAX} / 100) \times I_{TripMAX}$$

ee table 2 for $\%I_{TripMAX}$ at each step.)

s critical that the maximum rating (0.5 V) on the SENSE1 and NSE2 pins is not exceeded.

xed Off-Time. The internal PWM current control circuitry es a one-shot circuit to control the duration of time that the MOS FETs remain off. The off-time, t_{OFF}, is determined by the OSC terminal. The ROSC terminal has three settings:

- ROSC tied to VDD — off-time internally set to 30 µs, decay mode is automatic Mixed decay except when in full step where decay mode is set to Slow decay
- ROSC tied directly to ground — off-time internally set to 30 µs, current decay is set to Mixed decay for both increasing and decreasing currents, except in full step where decay mode is set to Slow decay. (See Low Current Microstepping section.)
- ROSC through a resistor to ground — off-time is determined by the following formula, the decay mode is automatic Mixed decay for all step modes.

$$t_{OFF} \approx R_{OSC} / 825$$

Where t_{OFF} is in µs.

Blanking. This function blanks the output of the current sense comparators when the outputs are switched by the internal current control circuitry. The comparator outputs are blanked to prevent false overcurrent detection due to reverse recovery currents of the clamp diodes, and switching transients related to the capacitance of the load. The blank time, t_{BLANK} (µs), is approximately

$$t_{BLANK} \approx 1 \text{ µs}$$

Shorted-Load and Short-to-Ground Protection. If the motor leads are shorted together, or if one of the leads is shorted to ground, the driver will protect itself by sensing the overcurrent event and disabling the driver that is shorted, protecting the device from damage. In the case of a short-to-ground, the device will remain disabled (latched) until the $\overline{SLEEP}$ input goes high or VDD power is removed. A short-to-ground overcurrent event is shown in figure 4.

When the two outputs are shorted together, the current path is through the sense resistor. After the blanking time (≈1 µs) expires, the sense resistor voltage is exceeding its trip value, due to the overcurrent condition that exists. This causes the driver to go into a fixed off-time cycle. After the fixed off-time expires the driver turns on again and the process repeats. In this condition the driver is completely protected against overcurrent events, but the short is repetitive with a period equal to the fixed off-time of the driver. This condition is shown in figure 5.

During a shorted load event it is normal to observe both a positive and negative current spike as shown in figure 3, due to the direction change implemented by the Mixed decay feature. This is shown in figure 6. In both instances the overcurrent circuitry is protecting the driver and prevents damage to the device.

Charge Pump (CP1 and CP2). The charge pump is used to generate a gate supply greater than that of VBB for driving the source-side FET gates. A 0.1 µF ceramic capacitor, should be connected between CP1 and CP2. In addition, a 0.1 µF ceramic capacitor is required between VCP and VBB, to act as a reservoir for operating the high-side FET gates.

Capacitor values should be Class 2 dielectric ±15% maximum, or tolerance R, according to EIA (Electronic Industries Alliance) specifications.

EG (VREG). This internally-generated voltage is used to erate the sink-side FET outputs. The VREG pin must be coupled with a 0.22 µF ceramic capacitor to ground. V_{REG} is ernally monitored. In the case of a fault condition, the FET puts of the A4988 are disabled.

pacitor values should be Class 2 dielectric ±15% maximum, tolerance R, according to EIA (Electronic Industries Alliance) cifications.

able Input (ENABLE). This input turns on or off all of the T outputs. When set to a logic high, the outputs are disabled. en set to a logic low, the internal control enables the outputs required. The translator inputs STEP, DIR, and MSx, as well as internal sequencing logic, all remain active, independent of the ABLE input state.

utdown. In the event of a fault, overtemperature (excess T_J) an undervoltage (on VCP), the FET outputs of the A4988 are abled until the fault condition is removed. At power-on, the LO (undervoltage lockout) circuit disables the FET outputs l resets the translator to the Home state.

eep Mode (SLEEP). To minimize power consumption en the motor is not in use, this input disables much of the ernal circuitry including the output FETs, current regulator, l charge pump. A logic low on the SLEEP pin puts the A4988 o Sleep mode. A logic high allows normal operation, as well as rt-up (at which time the A4988 drives the motor to the Home crostep position). When emerging from Sleep mode, in order allow the charge pump to stabilize, provide a delay of 1 ms fore issuing a Step command.

xed Decay Operation. The bridge operates in Mixed cay mode, depending on the step sequence, as shown in fig- s 8 through 12. As the trip point is reached, the A4988 initially es into a fast decay mode for 31.25% of the off-time, t_{OFF}. ter that, it switches to Slow Decay mode for the remainder of F. A timing diagram for this feature appears in figure 7.

nchronous Rectification. When a PWM-off cycle is ggered by an internal fixed-off time cycle, load current recircu- es according to the decay mode selected by the control logic. is synchronous rectification feature turns on the appropriate Ts during current decay, and effectively shorts out the body des with the low FET $R_{DS(ON)}$. This reduces power dissipation nificantly, and can eliminate the need for external Schottky des in many applications. Synchronous rectification turns off en the load current approaches zero (0 A), preventing reversal the load current.

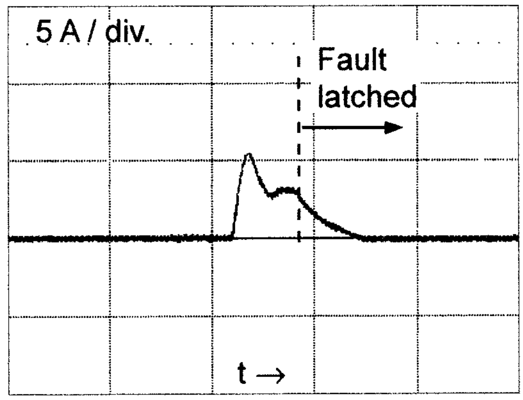


Figure 4. Short-to-ground event

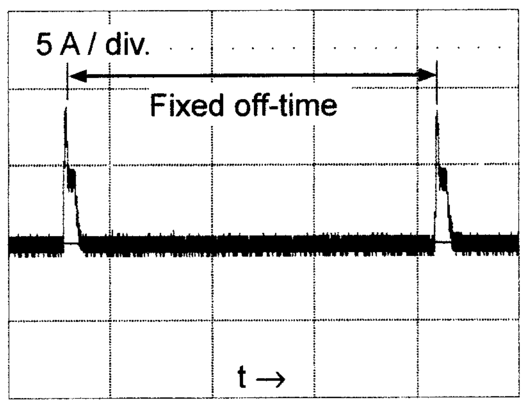


Figure 5. Shorted load (OUTxA → OUTxB) in Slow decay mode

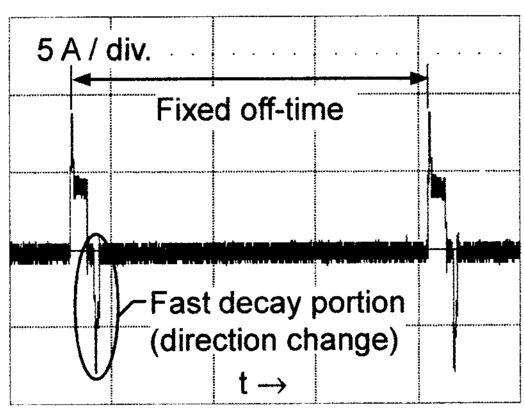
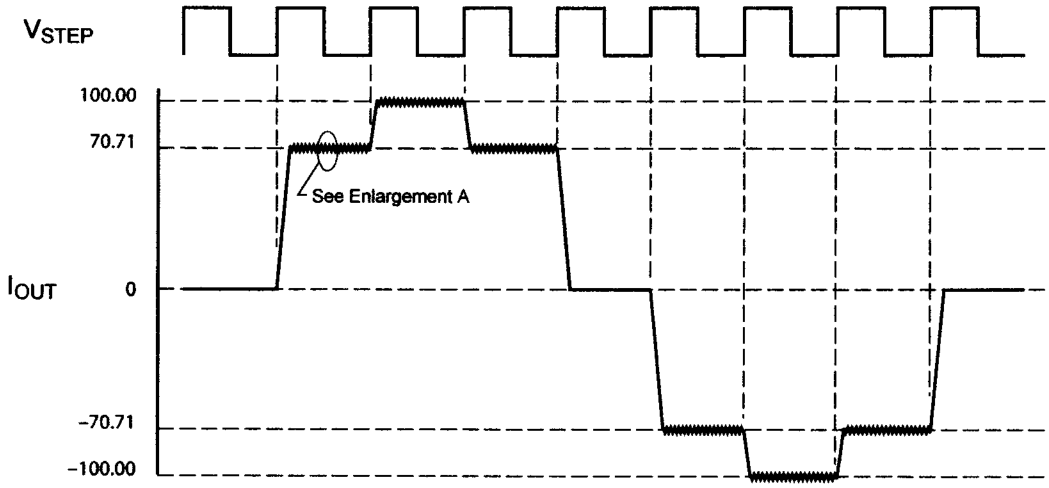
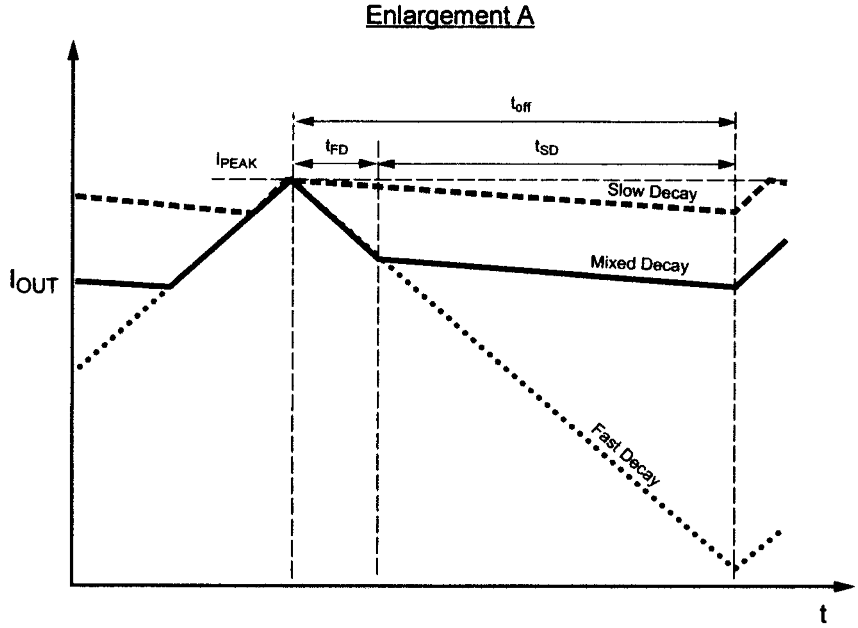


Figure 6. Shorted load (OUTxA → OUTxB) in Mixed decay mode





Symbol	Characteristic
t_{off}	Device fixed off-time
I_{PEAK}	Maximum output current
t_{SD}	Slow decay interval
t_{FD}	Fast decay interval
I_{OUT}	Device output current

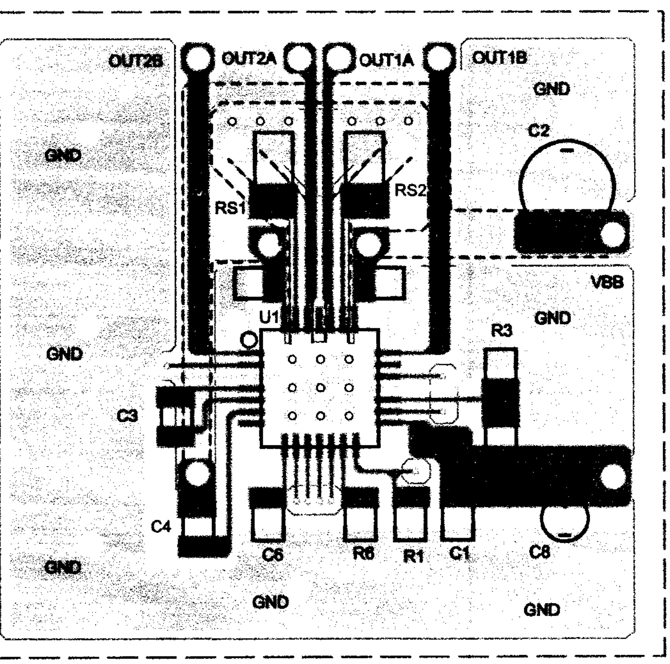
Figure 7. Current Decay Modes Timing Chart

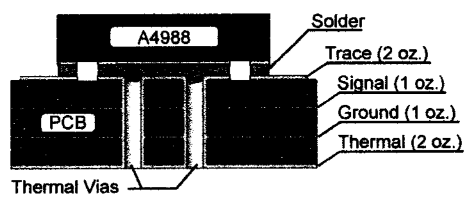
Application Layout

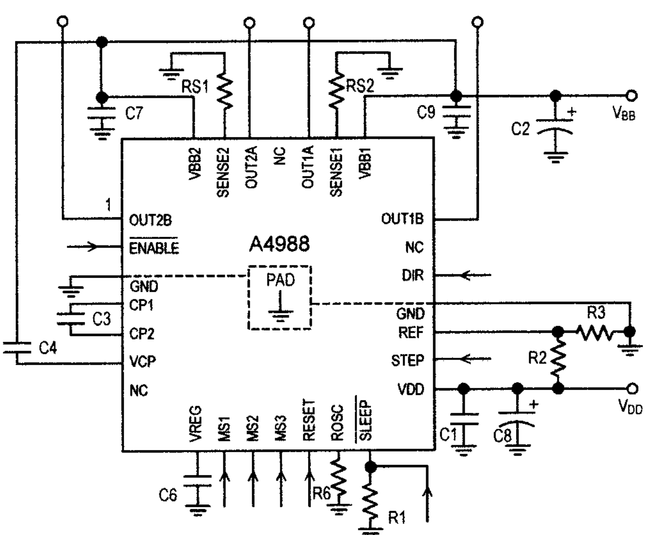
yout. The printed circuit board should use a heavy ground-ıne. For optimum electrical and thermal performance, the 988 must be soldered directly onto the board. Pins 3 and 18 internally fused, which provides a path for enhanced thermal sipation. Theses pins should be soldered directly to an exposed face on the PCB that connects to thermal vias are used to nsfer heat to other layers of the PCB.

order to minimize the effects of ground bounce and offset ues, it is important to have a low impedance single-point ound, known as a *star ground*, located very close to the device. making the connection between the pad and the ground plane ectly under the A4988, that area becomes an ideal location for tar ground point. A low impedance ground will prevent ground unce during high current operation and ensure that the supply ltage remains stable at the input terminal.

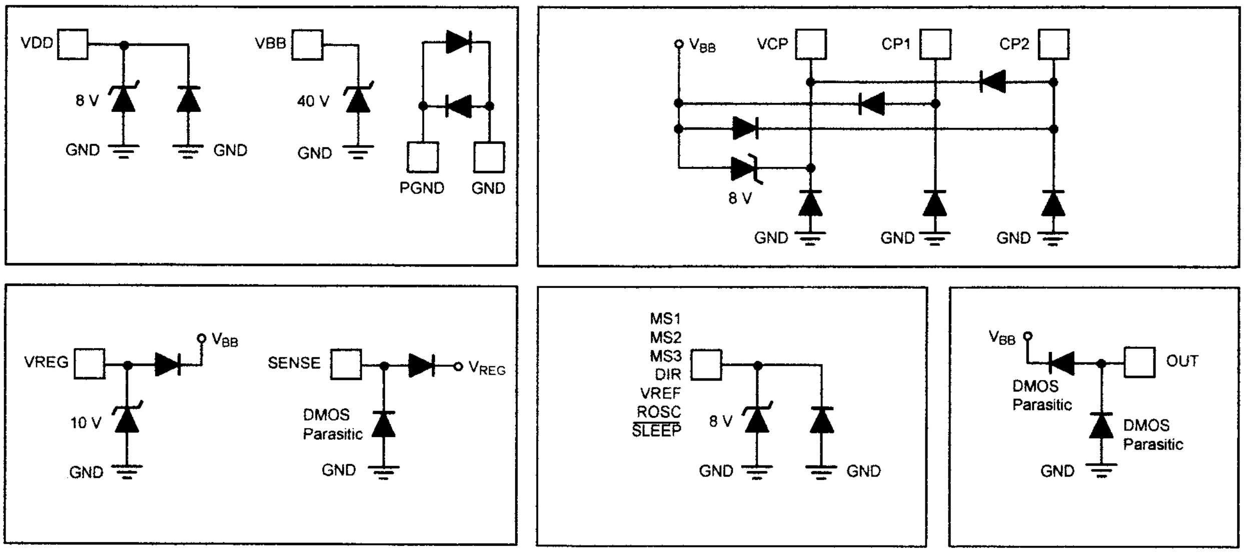
The two input capacitors should be placed in parallel, and as close to the device supply pins as possible. The ceramic capacitor (CIN1) should be closer to the pins than the bulk capacitor (CIN2). This is necessary because the ceramic capacitor will be responsible for delivering the high frequency current components. The sense resistors, RSx, should have a very low impedance path to ground, because they must carry a large current while supporting very accurate voltage measurements by the current sense comparators. Long ground traces will cause additional voltage drops, adversely affecting the ability of the comparators to accurately measure the current in the windings. The SENSEx pins have very short traces to the RSx resistors and very thick, low impedance traces directly to the star ground underneath the device. If possible, there should be no other components on the sense circuits.







Pin Circuit Diagrams



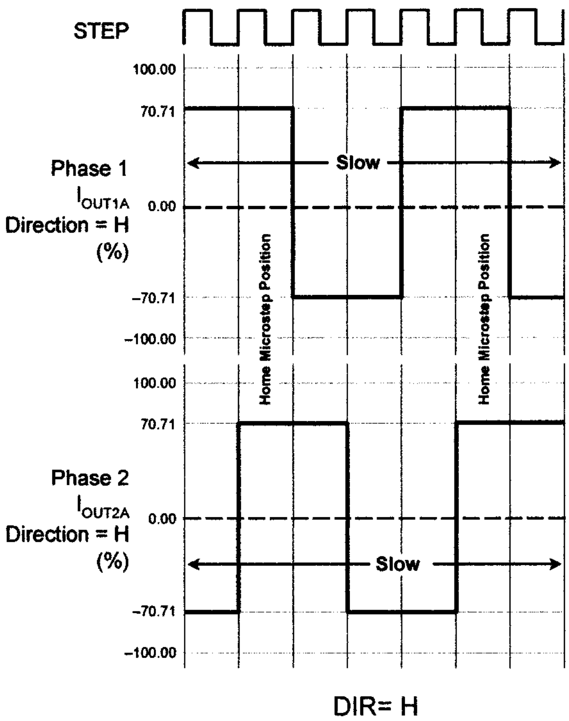


Figure 8. Decay Mode for Full-Step Increments

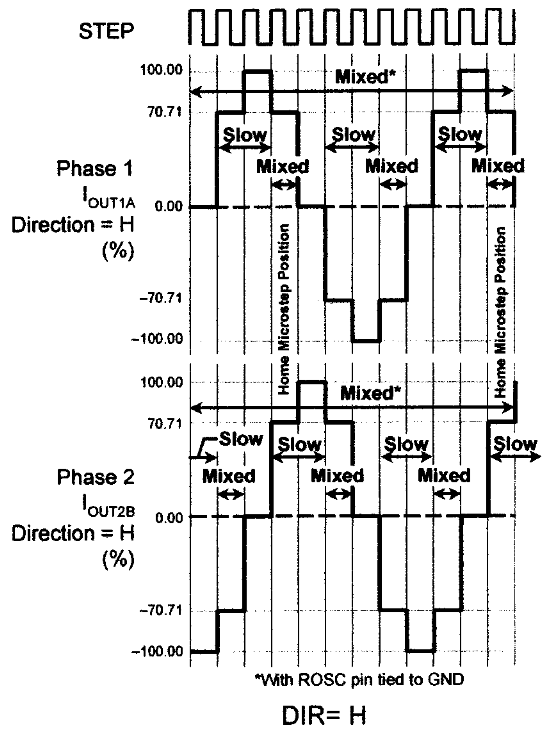


Figure 9. Decay Modes for Half-Step Increments

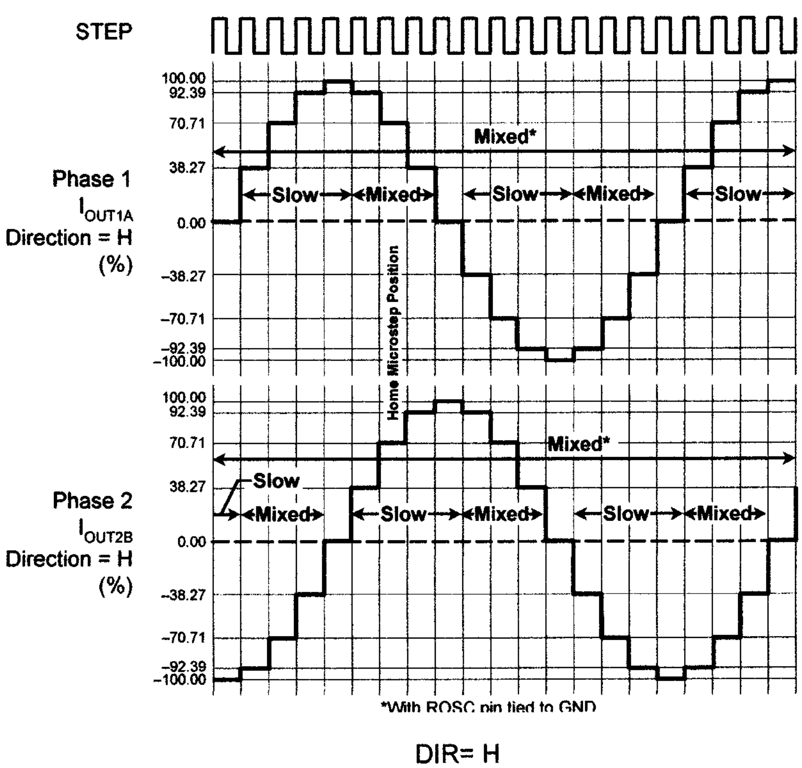


Figure 10. Decay Modes for Quarter-Step Increments

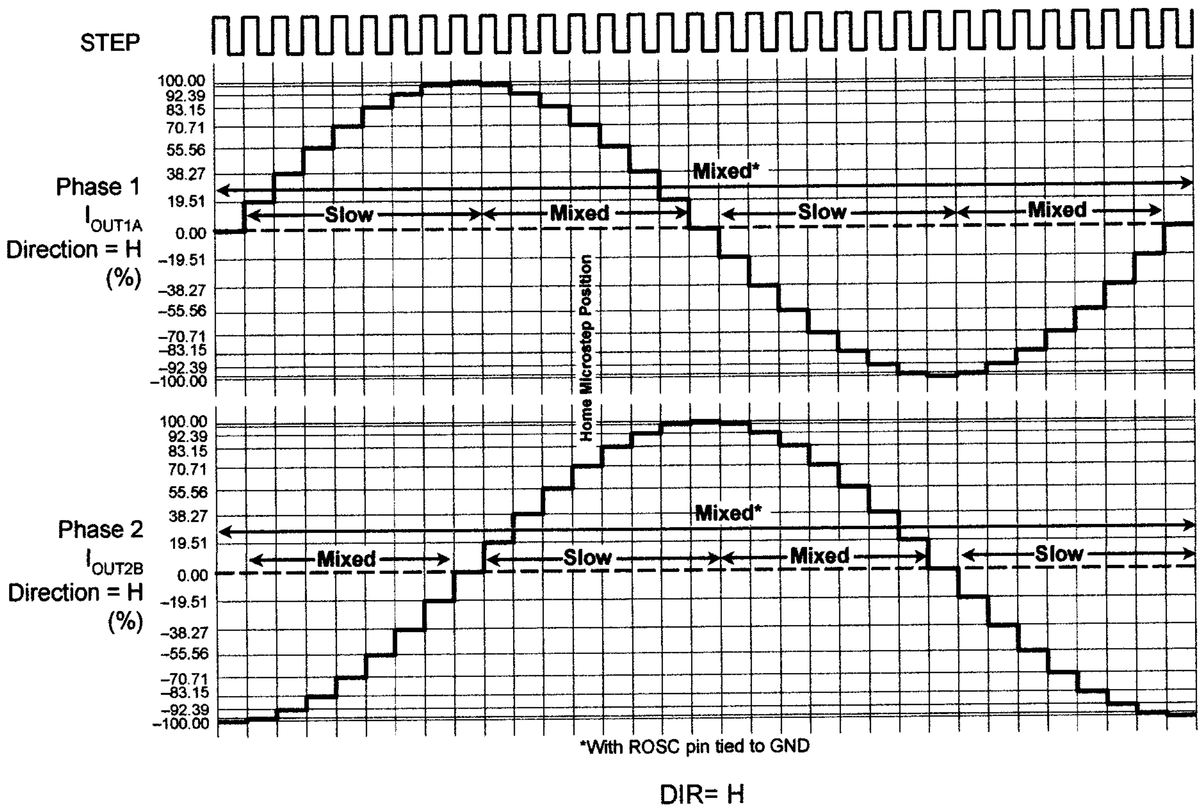


Figure 11. Decay Modes for Eighth-Step Increments

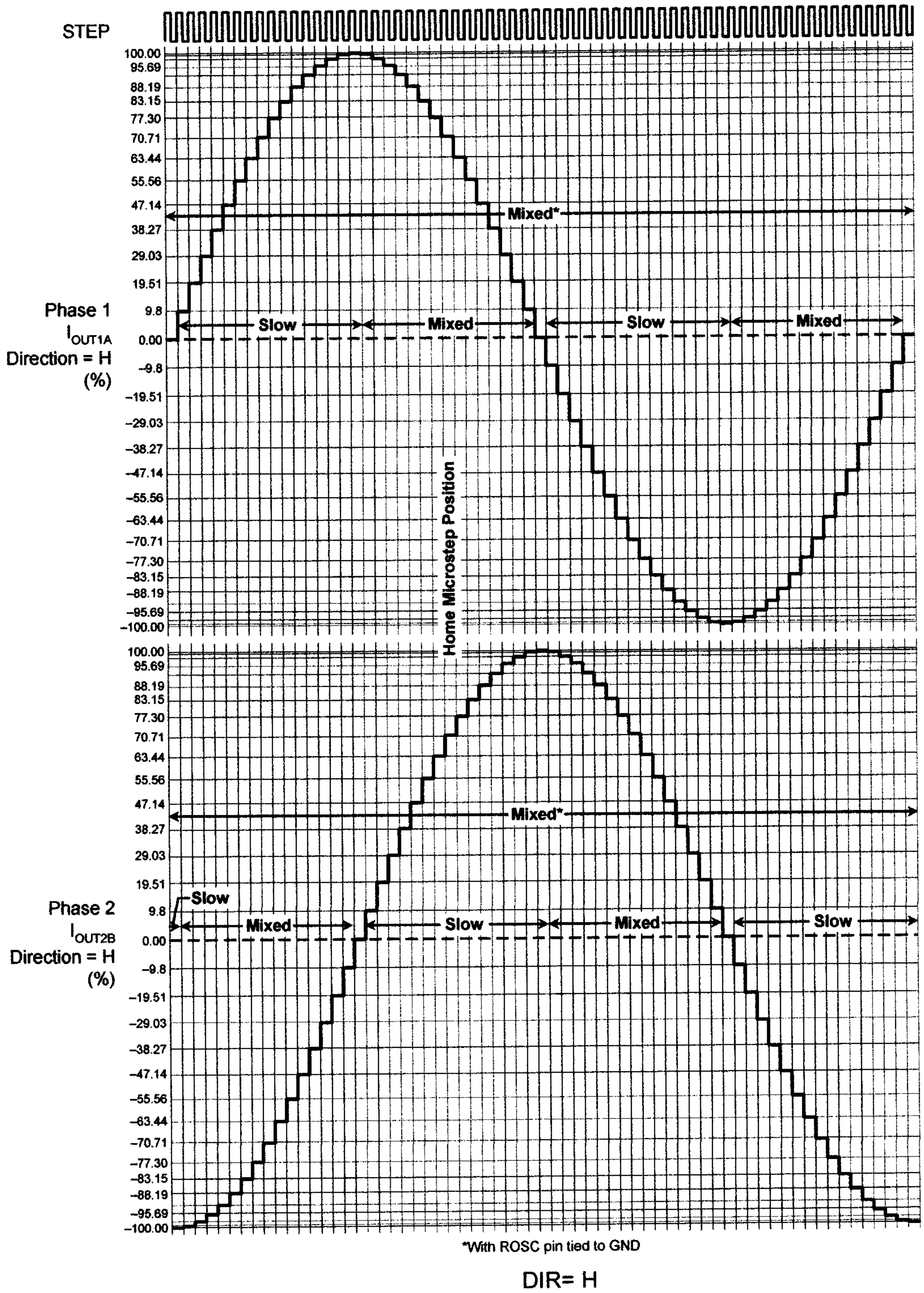


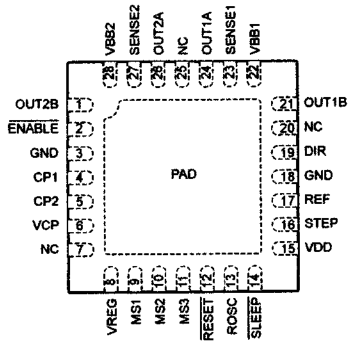
Figure 12. Decay Modes for Sixteenth-Step Increments

ble 2. Step Sequencing Settings

me microstep position at Step Angle 45°; DIR = H

ull tep #	Half Step #	1/4 Step #	1/8 Step #	1/16 Step #	Phase 1 Current [% $I_{tripMax}$] (%)	Phase 2 Current [% $I_{tripMax}$] (%)	Step Angle (°)	Full Step #	Half Step #	1/4 Step #	1/8 Step #	1/16 Step #	Phase 1 Current [% $I_{tripMax}$] (%)	Phase 2 Current [% $I_{tripMax}$] (%)	Step Angle (°)
	1	1	2	1	100.00	0.00	0.0		5	9	17	33	−100.00	0.00	180.0
				2	99.52	9.80	5.6					34	−99.52	−9.80	185.6
			2	3	98.08	19.51	11.3				18	35	−98.08	−19.51	191.3
				4	95.69	29.03	16.9					36	−95.69	−29.03	196.9
		2	3	5	92.39	38.27	22.5			10	19	37	−92.39	−38.27	202.5
				6	88.19	47.14	28.1					38	−88.19	−47.14	208.1
			4	7	83.15	55.56	33.8				20	39	−83.15	−55.56	213.8
				8	77.30	63.44	39.4					40	−77.30	−63.44	219.4
1	2	3	5	9	70.71	70.71	45.0	3	6	11	21	41	−70.71	−70.71	225.0
				10	63.44	77.30	50.6					42	−63.44	−77.30	230.6
			6	11	55.56	83.15	56.3				22	43	−55.56	−83.15	236.3
				12	47.14	88.19	61.9					44	−47.14	−88.19	241.9
		4	7	13	38.27	92.39	67.5			12	23	45	−38.27	−92.39	247.5
				14	29.03	95.69	73.1					46	−29.03	−95.69	253.1
			8	15	19.51	98.08	78.8				24	47	−19.51	−98.08	258.8
				16	9.80	99.52	84.4					48	−9.80	−99.52	264.4
	3	5	9	17	0.00	100.00	90.0		7	13	25	49	0.00	−100.00	270.0
				18	−9.80	99.52	95.6					50	9.80	−99.52	275.6
			10	19	−19.51	98.08	101.3				26	51	19.51	−98.08	281.3
				20	−29.03	95.69	106.9					52	29.03	−95.69	286.9
		6	11	21	−38.27	92.39	112.5			14	27	53	38.27	−92.39	292.5
				22	−47.14	88.19	118.1					54	47.14	−88.19	298.1
			12	23	−55.56	83.15	123.8				28	55	55.56	−83.15	303.8
				24	−63.44	77.30	129.4					56	63.44	−77.30	309.4
2	4	7	13	25	−70.71	70.71	135.0	4	8	15	29	57	70.71	−70.71	315.0
				26	−77.30	63.44	140.6					58	77.30	−63.44	320.6
			14	27	−83.15	55.56	146.3				30	59	83.15	−55.56	326.3
				28	−88.19	47.14	151.9					60	88.19	−47.14	331.9
		8	15	29	−92.39	38.27	157.5			16	31	61	92.39	−38.27	337.5
				30	−95.69	29.03	163.1					62	95.69	−29.03	343.1
			16	31	−98.08	19.51	168.8				32	63	98.08	−19.51	348.8
				32	−99.52	9.80	174.4					64	99.52	−9.80	354.4

Pin-out Diagram

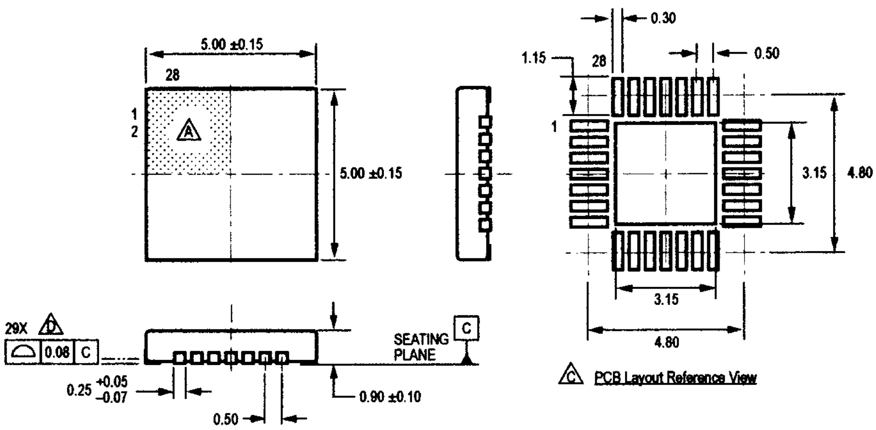


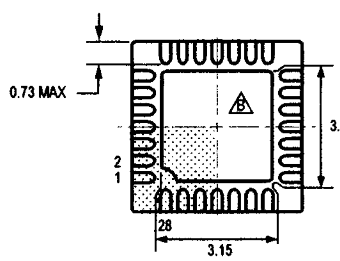
Terminal List Table

Name	Number	Description
CP1	4	Charge pump capacitor terminal
CP2	5	Charge pump capacitor terminal
VCP	6	Reservoir capacitor terminal
VREG	8	Regulator decoupling terminal
MS1	9	Logic input
MS2	10	Logic input
MS3	11	Logic input
$\overline{\text{RESET}}$	12	Logic input
ROSC	13	Timing set
$\overline{\text{SLEEP}}$	14	Logic input
VDD	15	Logic supply
STEP	16	Logic input
REF	17	G_m reference voltage input
GND	3, 18	Ground*
DIR	19	Logic input
OUT1B	21	DMOS Full Bridge 1 Output B
VBB1	22	Load supply
SENSE1	23	Sense resistor terminal for Bridge 1
OUT1A	24	DMOS Full Bridge 1 Output A
OUT2A	26	DMOS Full Bridge 2 Output A
SENSE2	27	Sense resistor terminal for Bridge 2
VBB2	28	Load supply
OUT2B	1	DMOS Full Bridge 2 Output B
$\overline{\text{ENABLE}}$	2	Logic input
NC	7, 20, 25	No connection
PAD	–	Exposed pad for enhanced thermal dissipation*

*The GND pins must be tied together externally by connecting to the PAD ground plane under the device.

ET Package, 28-Pin QFN with Exposed Thermal Pad





For Reference Only; not for tooling use
(reference JEDEC MO-220VHHD-1)
Dimensions in millimeters
Exact case and lead configuration at supplier discretion within limits shown

A Terminal #1 mark area

B Exposed thermal pad (reference only, terminal #1 identifier appearance at supplier discretion)

C Reference land pattern layout (reference IPC7351 QFN50P500X500X100-29V1M);
All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

D Coplanarity includes exposed thermal pad and terminals

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