Lampiran 1 : *Datasheet* Mikrokontroler AVR ATMega 8535

Features

- High-performance, Low-power AVR® 8-bit Microcontroller
- Advanced RISC Architecture
  - 130 Powerful Instructions – Most Single Clock Cycle Execution
  - 32 x 8 General Purpose Working Registers
  - Fully Static Operation
  - Up to 16 MIPS Throughput at 16 MHz
  - On-chip 2-cycle Multiplier
- Nonvolatile Program and Data Memories
  - 8K Bytes of In-System Self-Programmable Flash
    Endurance: 10,000 Write/Erase Cycles
  - Optional Boot Code Section with Independent Lock Bits
    In-System Programming by On-chip Boot Program
    True Read-While-Write Operation
  - 512 Bytes EEPROM
    Endurance: 100,000 Write/Erase Cycles
  - 512 Bytes Internal SRAM
  - Programming Lock for Software Security
- Peripheral Features
  - Two 8-bit Timer/Counters with Separate Prescalers and Compare Modes
  - One 16-bit Timer/Counter with Separate Prescaler, Compare Mode, and Capture Mode
  - Real Time Counter with Separate Oscillator
  - Four PWM Channels
  - 8-channel, 10-bit ADC
    8 Single-ended Channels
    7 Differential Channels for TQFP Package Only
    2 Differential Channels with Programmable Gain at 1x, 10x, or 200x for TQFP Package Only
  - Byte-oriented Two-wire Serial Interface
  - Programmable Serial USART
  - Master/Slave SPI Serial Interface
  - Programmable Watchdog Timer with Separate On-chip Oscillator
  - On-chip Analog Comparator
- Special Microcontroller Features
  - Power-on Reset and Programmable Brown-out Detection
  - Internal Calibrated RC Oscillator
  - External and Internal Interrupt Sources
  - Six Sleep Modes: Idle, ADC Noise Reduction, Power-save, Power-down, Standby and Extended Standby
- I/O and Packages
  - 32 Programmable I/O Lines
  - 40-pin PDIP, 44-lead TQFP, 44-lead PLCC, and 44-pad QFN/MLF
- Operating Voltages
  - 2.7 - 5.5V for ATmega8535L
  - 4.5 - 5.5V for ATmega8535
- Speed Grades
  - 0 - 8 MHz for ATmega8535L
  - 0 - 16 MHz for ATmega8535

8-bit AVR® Microcontroller with 8K Bytes In-System Programmable Flash

ATmega8535
ATmega8535L

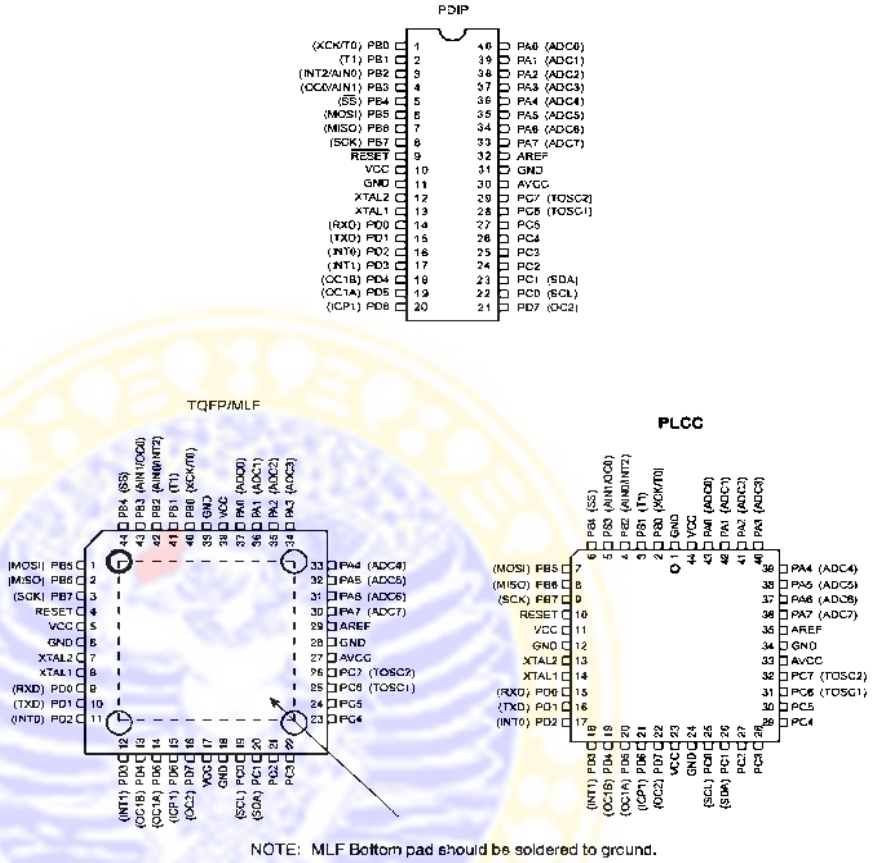
Summary

2502KS–AVR–10/06

Note: This is a summary document. A complete document is available on our Web site at www.atmel.com.

Pin Configurations

Figure 1. Pinout ATmega8535



Disclaimer

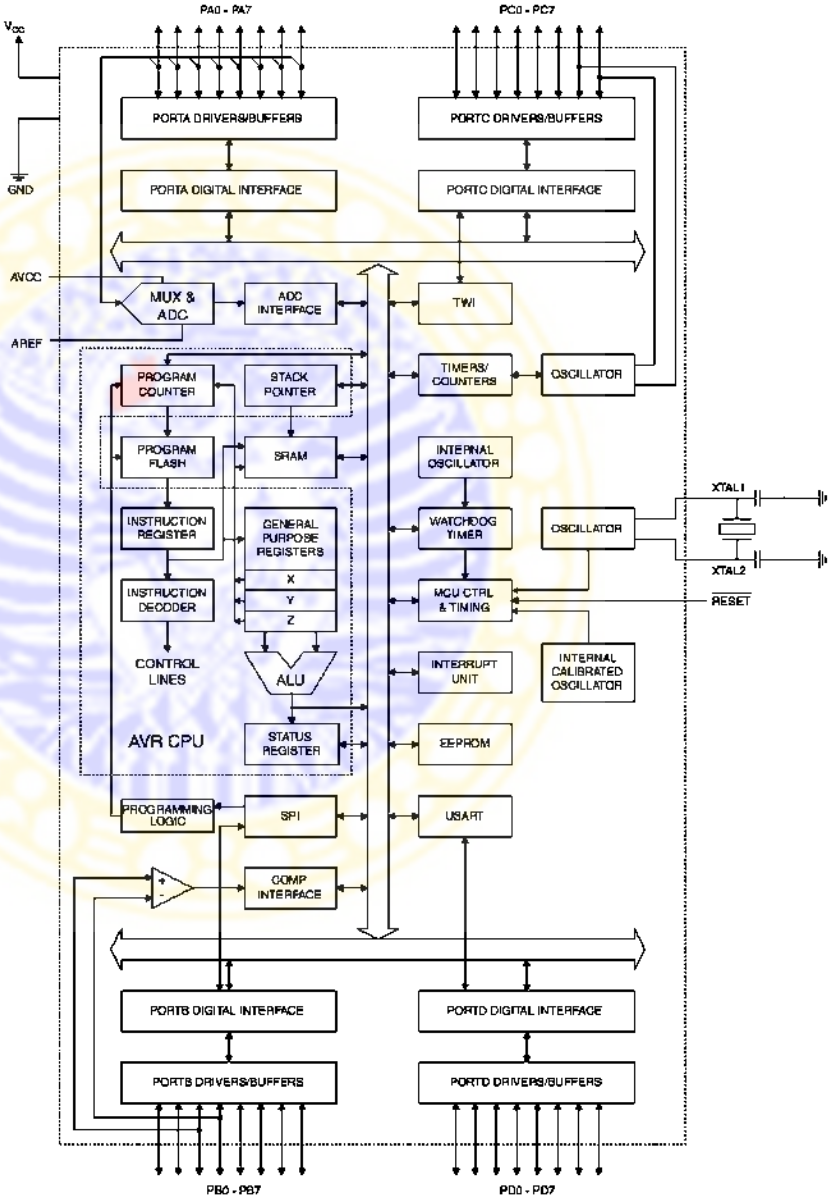
Typical values contained in this data sheet are based on simulations and characterization of other AVR microcontrollers manufactured on the same process technology. Min and Max values will be available after the device is characterized.

Overview

The ATmega8535 is a low-power CMOS 8-bit microcontroller based on the AVR enhanced RISC architecture. By executing instructions in a single clock cycle, the ATmega8535 achieves throughputs approaching 1 MIPS per MHz allowing the system designer to optimize power consumption versus processing speed.

Block Diagram

Figure 2. Block Diagram



The AVR core combines a rich instruction set with 32 general purpose working registers. All 32 registers are directly connected to the Arithmetic Logic Unit (ALU), allowing two independent registers to be accessed in one single instruction executed in one clock cycle. The resulting architecture is more code efficient while achieving throughputs up to ten times faster than conventional CISC microcontrollers.

The ATmega8535 provides the following features: 8K bytes of In-System Programmable Flash with Read-While-Write capabilities, 512 bytes EEPROM, 512 bytes SRAM, 32 general purpose I/O lines, 32 general purpose working registers, three flexible Timer/Counters with compare modes, internal and external interrupts, a serial programmable USART, a byte oriented Two-wire Serial Interface, an 8-channel, 10-bit ADC with optional differential input stage with programmable gain in TQFP package, a programmable Watchdog Timer with Internal Oscillator, an SPI serial port, and six software selectable power saving modes. The Idle mode stops the CPU while allowing the SRAM, Timer/Counters, SPI port, and interrupt system to continue functioning. The Power-down mode saves the register contents but freezes the Oscillator, disabling all other chip functions until the next interrupt or Hardware Reset. In Power-save mode, the asynchronous timer continues to run, allowing the user to maintain a timer base while the rest of the device is sleeping. The ADC Noise Reduction mode stops the CPU and all I/O modules except asynchronous timer and ADC, to minimize switching noise during ADC conversions. In Standby mode, the crystal/resonator Oscillator is running while the rest of the device is sleeping. This allows very fast start-up combined with low-power consumption. In Extended Standby mode, both the main Oscillator and the asynchronous timer continue to run.

The device is manufactured using Atmel's high density nonvolatile memory technology. The On-chip ISP Flash allows the program memory to be reprogrammed In-System through an SPI serial interface, by a conventional nonvolatile memory programmer, or by an On-chip Boot program running on the AVR core. The boot program can use any interface to download the application program in the Application Flash memory. Software in the Boot Flash section will continue to run while the Application Flash section is updated, providing true Read-While-Write operation. By combining an 8-bit RISC CPU with In-System Self-Programmable Flash on a monolithic chip, the Atmel ATmega8535 is a powerful microcontroller that provides a highly flexible and cost effective solution to many embedded control applications.

The ATmega8535 AVR is supported with a full suite of program and system development tools including: C compilers, macro assemblers, program debugger/simulators, In-Circuit Emulators, and evaluation kits.

AT90S8535 Compatibility

The ATmega8535 provides all the features of the AT90S8535. In addition, several new features are added. The ATmega8535 is backward compatible with AT90S8535 in most cases. However, some incompatibilities between the two microcontrollers exist. To solve this problem, an AT90S8535 compatibility mode can be selected by programming the S8535C fuse. ATmega8535 is pin compatible with AT90S8535, and can replace the AT90S8535 on current Printed Circuit Boards. However, the location of fuse bits and the electrical characteristics differs between the two devices.

AT90S8535 Compatibility Mode

Programming the S8535C fuse will change the following functionality:

- The timed sequence for changing the Watchdog Time-out period is disabled. See "Timed Sequences for Changing the Configuration of the Watchdog Timer" on page 45 for details.
- The double buffering of the USART Receive Register is disabled. See "AVR USART vs. AVR UART – Compatibility" on page 146 for details.

Pin Descriptions

V_{CC}	Digital supply voltage.
GND	Ground.
Port A (PA7..PA0)	Port A serves as the analog inputs to the A/D Converter. Port A also serves as an 8-bit bi-directional I/O port, if the A/D Converter is not used. Port pins can provide internal pull-up resistors (selected for each bit). The Port A output buffers have symmetrical drive characteristics with both high sink and source capability. When pins PA0 to PA7 are used as inputs and are externally pulled low, they will source current if the internal pull-up resistors are activated. The Port A pins are tri-stated when a reset condition becomes active, even if the clock is not running.
Port B (PB7..PB0)	Port B is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port B output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port B pins that are externally pulled low will source current if the pull-up resistors are activated. The Port B pins are tri-stated when a reset condition becomes active, even if the clock is not running. Port B also serves the functions of various special features of the ATmega8535 as listed on page 60.
Port C (PC7..PC0)	Port C is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port C output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port C pins that are externally pulled low will source current if the pull-up resistors are activated. The Port C pins are tri-stated when a reset condition becomes active, even if the clock is not running.
Port D (PD7..PD0)	Port D is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port D output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port D pins that are externally pulled low will source current if the pull-up resistors are activated. The Port D pins are tri-stated when a reset condition becomes active, even if the clock is not running. Port D also serves the functions of various special features of the ATmega8535 as listed on page 64.
$\overline{\text{RESET}}$	Reset input. A low level on this pin for longer than the minimum pulse length will generate a reset, even if the clock is not running. The minimum pulse length is given in Table 15 on page 37. Shorter pulses are not guaranteed to generate a reset.
XTAL1	Input to the inverting Oscillator amplifier and input to the internal clock operating circuit.
XTAL2	Output from the inverting Oscillator amplifier.
AVCC	AVCC is the supply voltage pin for Port A and the A/D Converter. It should be externally connected to V_{CC}, even if the ADC is not used. If the ADC is used, it should be connected to V_{CC} through a low-pass filter.
AREF	AREF is the analog reference pin for the A/D Converter.

Lampiran 2 : *Datasheet* IC LM555

National Semiconductor

February 1995

LM555/LM555C Timer

General Description

The LM555 is a highly stable device for generating accurate time delays or oscillation. Additional terminals are provided for triggering or resetting if desired. In the time delay mode of operation, the time is precisely controlled by one external resistor and capacitor. For astable operation as an oscillator, the free running frequency and duty cycle are accurately controlled with two external resistors and one capacitor. The circuit may be triggered and reset on falling waveforms, and the output circuit can source or sink up to 200 mA or drive TTL circuits.

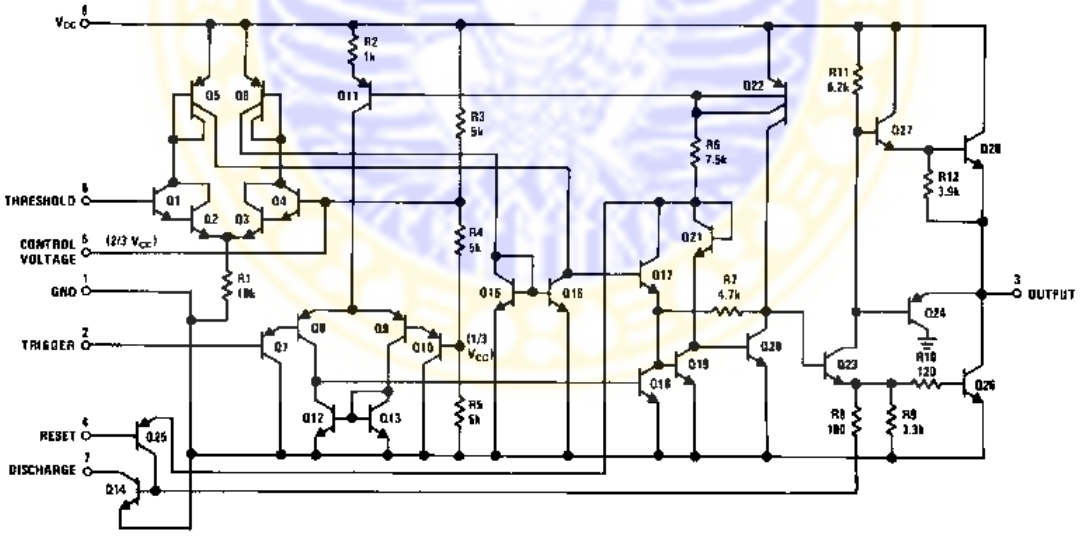
Features

- Direct replacement for SE555/NE555
- Timing from microseconds through hours
- Operates in both astable and monostable modes
- Adjustable duty cycle
- Output can source or sink 200 mA
- Output and supply TTL compatible
- Temperature stability better than 0.005% per °C
- Normally on and normally off output

Applications

- Precision timing
- Pulse generation
- Sequential timing
- Time delay generation
- Pulse width modulation
- Pulse position modulation
- Linear ramp generator

Schematic Diagram



TL/H/7851–1

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RRD-B30M115/Printed in U. S. A.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage +18V

Power Dissipation (Note 1)
- LM555H, LM555CH 760 mW
- LM555, LM555CN 1180 mW

Operating Temperature Ranges
- LM555C 0°C to +70°C
- LM555 −55°C to + 125°C

Storage Temperature Range −65°C to +150°C

Soldering Information
- Dual-In-Line Package
  - Soldering (10 Seconds) 260°C
- Small Outline Package
  - Vapor Phase (60 Seconds) 215°C
  - Infrared (15 Seconds) 220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

Electrical Characteristics (T_A = 25°C, V_{CC} = +5V to +15V, unless otherwise specified)

Parameter	Conditions	Limits						Units
		LM555			LM555C			
		Min	Typ	Max	Min	Typ	Max	
Supply Voltage		4.5		18	4.5		16	V
Supply Current	V_{CC} = 5V, R_L = ∞ V_{CC} = 15V, R_L = ∞ (Low State) (Note 2)		3 10	5 12		3 10	6 15	mA mA
Timing Error, Monostable								
Initial Accuracy			0.5			1		%
Drift with Temperature	R_A = 1k to 100 kΩ, C = 0.1 μF, (Note 3)		30			50		ppm/°C
Accuracy over Temperature			1.5			1.5		%
Drift with Supply			0.05			0.1		%/V
Timing Error, Astable								
Initial Accuracy			1.5			2.25		%
Drift with Temperature	R_A, R_B = 1k to 100 kΩ, C = 0.1 μF, (Note 3)		90			150		ppm/°C
Accuracy over Temperature			2.5			3.0		%
Drift with Supply			0.15			0.30		%/V
Threshold Voltage			0.667			0.667		x V_{CC}
Trigger Voltage	V_{CC} = 15V V_{CC} = 5V	4.8 1.45	5 1.67	5.2 1.9		5 1.67		V V
Trigger Current			0.01	0.5		0.5	0.9	μA
Reset Voltage		0.4	0.5	1	0.4	0.5	1	V
Reset Current			0.1	0.4		0.1	0.4	mA
Threshold Current	(Note 4)		0.1	0.25		0.1	0.25	μA
Control Voltage Level	V_{CC} = 15V V_{CC} = 5V	9.6 2.9	10 3.33	10.4 3.8	9 2.6	10 3.33	11 4	V V
Pin 7 Leakage Output High			1	100		1	100	nA
Pin 7 Sat (Note 5)								
Output Low	V_{CC} = 15V, I_7 = 15 mA		150			180		mV
Output Low	V_{CC} = 4.5V, I_7 = 4.5 mA		70	100		80	200	mV

Electrical Characteristics $T_A = 25°C$, $V_{CC} = +5V$ to $+15V$, (unless otherwise specified) (Continued)

Parameter	Conditions	Limits						Units
		LM555			LM555C			
		Min	Typ	Max	Min	Typ	Max	
Output Voltage Drop (Low)	$V_{CC} = 15V$							
	$I_{SINK} = 10$ mA		0.1	0.15		0.1	0.25	V
	$I_{SINK} = 50$ mA		0.4	0.5		0.4	0.75	V
	$I_{SINK} = 100$ mA		2	2.2		2	2.5	V
	$I_{SINK} = 200$ mA		2.5			2.5		V
	$V_{CC} = 5V$							
	$I_{SINK} = 8$ mA		0.1	0.25				V
	$I_{SINK} = 5$ mA					0.25	0.35	V
Output Voltage Drop (High)	$I_{SOURCE} = 200$ mA, $V_{CC} = 15V$		12.5			12.5		V
	$I_{SOURCE} = 100$ mA, $V_{CC} = 15V$	13	13.3		12.75	13.3		V
	$V_{CC} = 5V$	3	3.3		2.75	3.3		V
Rise Time of Output			100			100		ns
Fall Time of Output			100			100		ns

Note 1: For operating at elevated temperatures the device must be derated above 25°C based on a +150°C maximum junction temperature and a thermal resistance of 164°c/w (T0-5), 106°c/w (DIP) and 170°c/w (S0-8) junction to ambient.

Note 2: Supply current when output high typically 1 mA less at $V_{CC} = 5V$.

Note 3: Tested at $V_{CC} = 5V$ and $V_{CC} = 15V$.

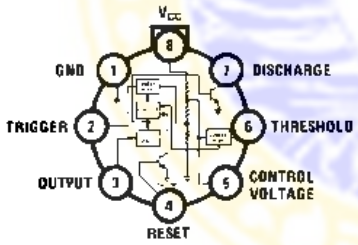
Note 4: This will determine the maximum value of $R_A + R_B$ for 15V operation. The maximum total ($R_A + R_B$) is 20 MΩ.

Note 5: No protection against excessive pin 7 current is necessary providing the package dissipation rating will not be exceeded.

Note 6: Refer to RETS555X drawing of military LM555H and LM555J versions for specifications.

Connection Diagrams

Metal Can Package



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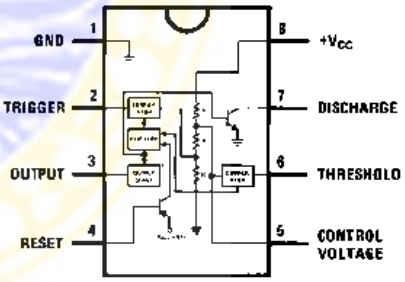
Top View

Order Number LM555H or LM555CH
See NS Package Number H08C

Dual-In-Line and Small Outline Packages



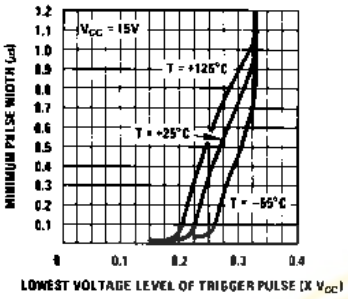
TL/H/7851–3

Top View

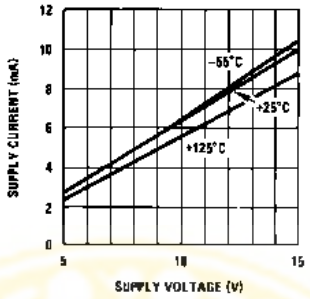
Order Number LM555J, LM555CJ,
LM555CM or LM555CN
See NS Package Number J08A, M08A or N08E

Typical Performance Characteristics

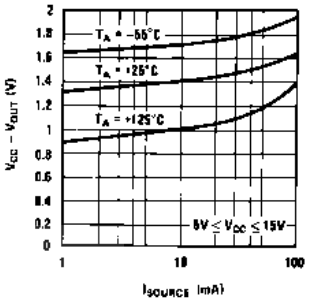
Minimuim Pulse Width Required for Triggering



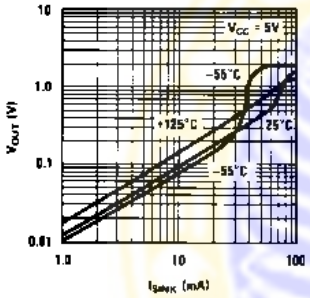
Supply Current vs Supply Voltage



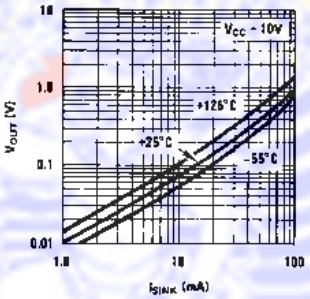
High Output Voltage vs Output Source Current



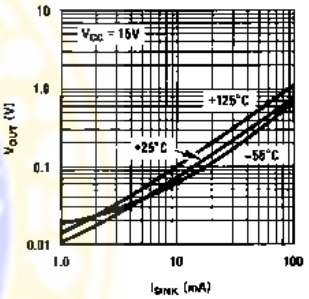
Low Output Voltage vs Output Sink Current



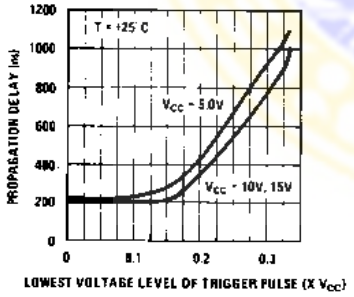
Low Output Voltage vs Output Sink Current



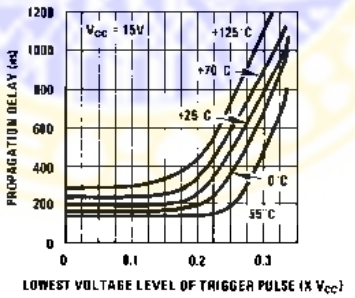
Low Output Voltage vs Output Sink Current



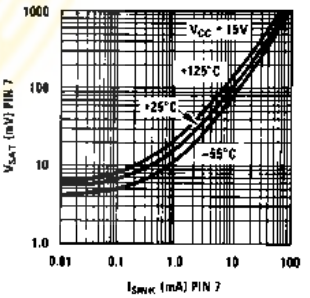
Output Propagation Delay vs Voltage Level of Trigger Pulse



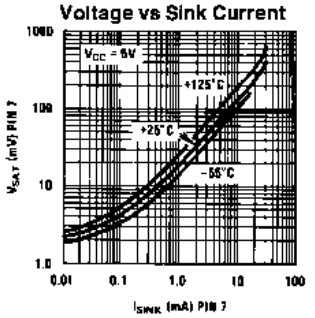
Output Propagation Delay vs Voltage Level of Trigger Pulse



Discharge Transistor (Pin 7) Voltage vs Sink Current



Discharge Transistor (Pin 7) Voltage vs Sink Current

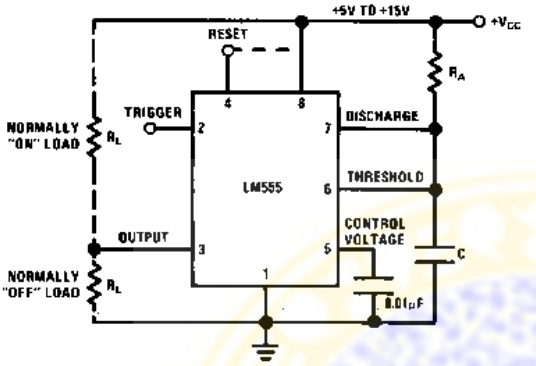


TL/H/7851–4

Applications Information

MONOSTABLE OPERATION

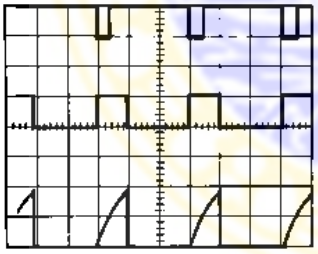
In this mode of operation, the timer functions as a one-shot *(Figure 1)*. The external capacitor is initially held discharged by a transistor inside the timer. Upon application of a negative trigger pulse of less than 1/3 V_{CC} to pin 2, the flip-flop is set which both releases the short circuit across the capacitor and drives the output high.



TL/H/7851–5

FIGURE 1. Monostable

The voltage across the capacitor then increases exponentially for a period of t = 1.1 R_A C, at the end of which time the voltage equals 2/3 V_{CC}. The comparator then resets the flip-flop which in turn discharges the capacitor and drives the output to its low state. *Figure 2* shows the waveforms generated in this mode of operation. Since the charge and the threshold level of the comparator are both directly proportional to supply voltage, the timing internal is independent of supply.



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V_{CC} = 5V
TIME = 0.1 ms/DIV.
R_A = 9.1 kΩ
C = 0.01 μF

Top Trace: Input 5V/Div.
Middle Trace: Output 5V/Div.
Bottom Trace: Capacitor Voltage 2V/Div.

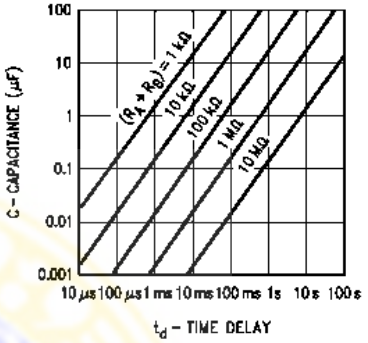
FIGURE 2. Monostable Waveforms

During the timing cycle when the output is high, the further application of a trigger pulse will not effect the circuit so long as the trigger input is returned high at least 10 μs before the end of the timing interval. However the circuit can be reset during this time by the application of a negative pulse to the reset terminal (pin 4). The output will then remain in the low state until a trigger pulse is again applied.

When the reset function is not in use, it is recommended that it be connected to V_{CC} to avoid any possibility of false triggering.

Figure 3 is a nomograph for easy determination of R, C values for various time delays.

NOTE: In monostable operation, the trigger should be driven high before the end of timing cycle.

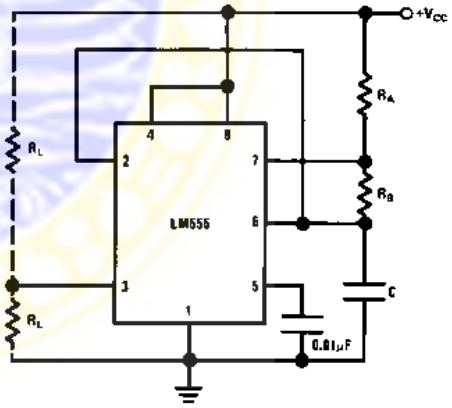


TL/H/7851–7

FIGURE 3. Time Delay

ASTABLE OPERATION

If the circuit is connected as shown in *Figure 4* (pins 2 and 6 connected) it will trigger itself and free run as a multivibrator. The external capacitor charges through R_A + R_B and discharges through R_B. Thus the duty cycle may be precisely set by the ratio of these two resistors.



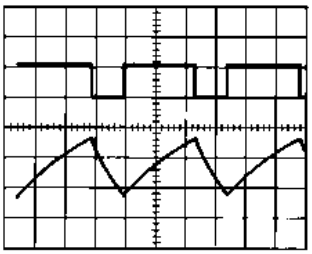
TL/H/7851–8

FIGURE 4. Astable

In this mode of operation, the capacitor charges and discharges between 1/3 V_{CC} and 2/3 V_{CC}. As in the triggered mode, the charge and discharge times, and therefore the frequency are independent of the supply voltage.

Applications Information (Continued)

Figure 5 shows the waveforms generated in this mode of operation.



TL/H/7851–8

V_{CC} = 5V
TIME = 20 μs/DIV.
R_A = 3.9 kΩ
R_B = 3 kΩ
C = 0.01 μF

Top Trace: Output 5V/Div.
Bottom Trace: Capacitor Voltage 1V/Div.

FIGURE 5. Astable Waveforms

The charge time (output high) is given by:

$$t_1 = 0.693\ (R_A + R_B)\ C$$

And the discharge time (output low) by:

$$t_2 = 0.693\ (R_B)\ C$$

Thus the total period is:

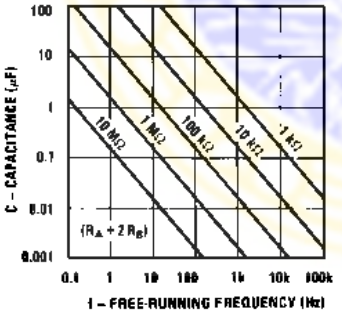
$$T = t_1 + t_2 = 0.693\ (R_A + 2R_B)\ C$$

The frequency of oscillation is:

$$f = \frac{1}{T} = \frac{1.44}{(R_A + 2R_B)\ C}$$

Figure 6 may be used for quick determination of these RC values.

The duty cycle is: $D = \dfrac{R_B}{R_A + 2R_B}$

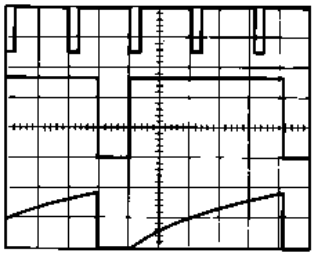


TL/H/7851–10

FIGURE 6. Free Running Frequency

FREQUENCY DIVIDER

The monostable circuit of *Figure 1* can be used as a frequency divider by adjusting the length of the timing cycle. *Figure 7* shows the waveforms generated in a divide by three circuit.



TL/H/7851–11

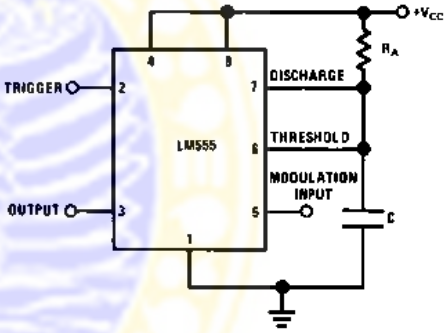
V_{CC} = 5V
TIME = 20 μs/DIV.
R_A = 9.1 kΩ
C = 0.01 μF

Top Trace: Input 4V/Div.
Middle Trace: Output 2V/Div.
Bottom Trace: Capacitor 2V/Div.

FIGURE 7. Frequency Divider

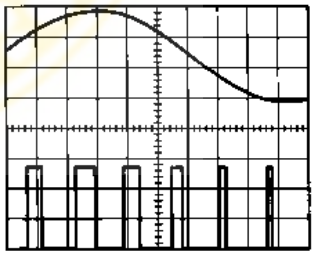
PULSE WIDTH MODULATOR

When the timer is connected in the monostable mode and triggered with a continuous pulse train, the output pulse width can be modulated by a signal applied to pin 5. *Figure 8* shows the circuit, and in *Figure 9* are some waveform examples.



TL/H/7851–12

FIGURE 8. Pulse Width Modulator



TL/H/7851–13

V_{CC} = 5V
TIME = 0.2 ms/DIV.
R_A = 9.1 kΩ
C = 0.01 μF

Top Trace: Modulation 1V/Div.
Bottom Trace: Output Voltage 2V/Div.

FIGURE 9. Pulse Width Modulator

PULSE POSITION MODULATOR

This application uses the timer connected for astable operation, as in *Figure 10*, with a modulating signal again applied to the control voltage terminal. The pulse position varies with the modulating signal, since the threshold voltage and hence the time delay is varied. *Figure 11* shows the waveforms generated for a triangle wave modulation signal.

Lampiran 3 : *Datasheet* IC 4001

National Semiconductor

March 1988

CD4001BM/CD4001BC Quad 2-Input NOR Buffered B Series Gate
CD4011BM/CD4011BC Quad 2-Input NAND Buffered B Series Gate

CD4001BM/CD4001BC Quad 2-Input NOR Buffered B Series Gate
CD4011BM/CD4011BC Quad 2-Input NAND Buffered B Series Gate

General Description

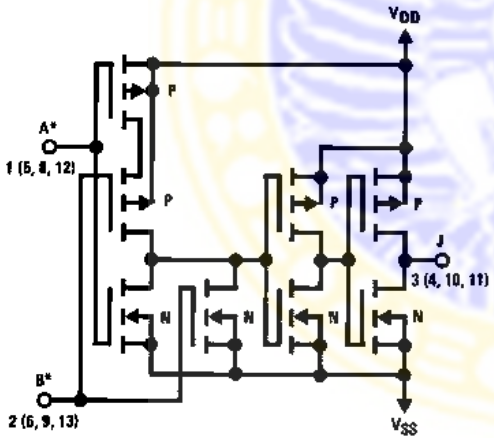
These quad gates are monolithic complementary MOS (CMOS) integrated circuits constructed with N- and P-channel enhancement mode transistors. They have equal source and sink current capabilities and conform to standard B series output drive. The devices also have buffered outputs which improve transfer characteristics by providing very high gain.

All inputs are protected against static discharge with diodes to V_{DD} and V_{SS}.

Features

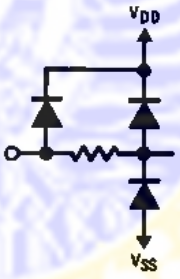
- Low power TTL compatibility — Fan out of 2 driving 74L or 1 driving 74LS
- 5V–10V–15V parametric ratings
- Symmetrical output characteristics
- Maximum input leakage 1 μA at 15V over full temperature range

Schematic Diagrams



TL/F/5939–1

CD4001BC/BM



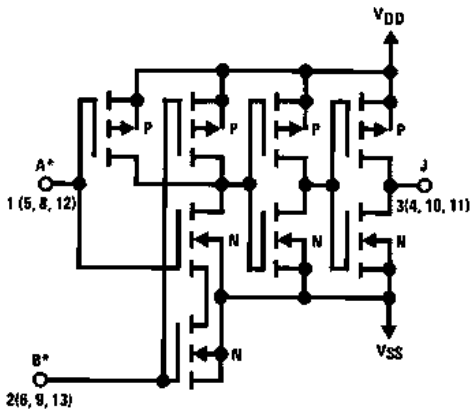
¼ of device shown

$J = \overline{A + B}$

Logical "1" = High
Logical "0" = Low

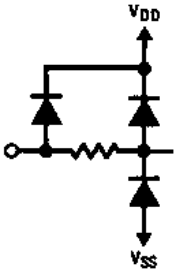
TL/F/5939–2

*All inputs protected by standard CMOS protection circuit.



TL/F/5939–5

CD4011BC/BM



¼ of device shown

$J = \overline{A \cdot B}$

Logical "1" = High
Logical "0" = Low

TL/F/5939–6

*All inputs protected by standard CMOS protection circuit.

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RRD-B30M105/Printed in U. S. A.

Absolute Maximum Ratings (Notes 1 and 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Voltage at any Pin	−0.5V to V_{DD} +0.5V
Power Dissipation (P_D)	
Dual-In-Line	700 mW
Small Outline	500 mW
V_{DD} Range	−0.5 V_{DC} to +18 V_{DC}
Storage Temperature (T_S)	−65°C to +150°C
Lead Temperature (T_L) (Soldering, 10 seconds)	260°C

Operating Conditions

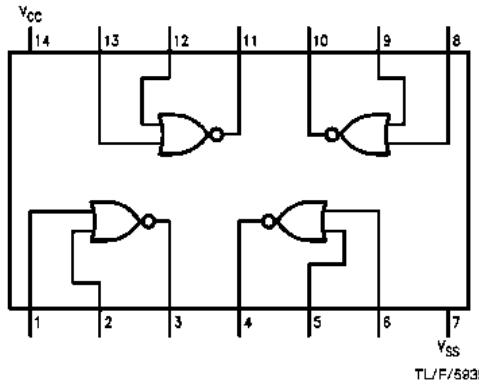
Operating Range (V_{DD})	3 V_{DC} to 15 V_{DC}
Operating Temperature Range	
CD4001BM, CD4011BM	−55°C to +125°C
CD4001BC, CD4011BC	−40°C to +85°C

DC Electrical Characteristics CD4001BM, CD4011BM (Note 2)

Symbol	Parameter	Conditions	−55°C		+25°C			+125°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	V_{DD} = 5V, V_{IN} = V_{DD} or V_{SS}		0.25		0.004	0.25		7.5	μA
		V_{DD} = 10V, V_{IN} = V_{DD} or V_{SS}		0.50		0.005	0.50		15	μA
		V_{DD} = 15V, V_{IN} = V_{DD} or V_{SS}		1.0		0.006	1.0		30	μA
V_{OL}	Low Level Output Voltage	V_{DD} = 5V, I_O < 1 μA		0.05		0	0.05		0.05	V
		V_{DD} = 10V, I_O < 1 μA		0.05		0	0.05		0.05	V
		V_{DD} = 15V, I_O < 1 μA		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	V_{DD} = 5V, I_O < 1 μA	4.95		4.95	5		4.95		V
		V_{DD} = 10V, I_O < 1 μA	9.95		9.95	10		9.95		V
		V_{DD} = 15V, I_O < 1 μA	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	V_{DD} = 5V, V_O = 4.5V		1.5		2	1.5		1.5	V
		V_{DD} = 10V, V_O = 9.0V		3.0		4	3.0		3.0	V
		V_{DD} = 15V, V_O = 13.5V		4.0		6	4.0		4.0	V
V_{IH}	High Level Input Voltage	V_{DD} = 5V, V_O = 0.5V	3.5		3.5	3		3.5		V
		V_{DD} = 10V, V_O = 1.0V	7.0		7.0	6		7.0		V
		V_{DD} = 15V, V_O = 1.5V	11.0		11.0	9		11.0		V
I_{OL}	Low Level Output Current (Note 3)	V_{DD} = 5V, V_O = 0.4V	0.64		0.51	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.6		1.3	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	4.2		3.4	8.8		2.4		mA
I_{OH}	High Level Output Current (Note 3)	V_{DD} = 5V, V_O = 4.6V	−0.64		−0.51	−0.88		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.6		−1.3	−2.25		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−4.2		−3.4	−8.8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.10		-10^{-5}	−0.10		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.10		10^{-5}	0.10		1.0	μA

Connection Diagrams

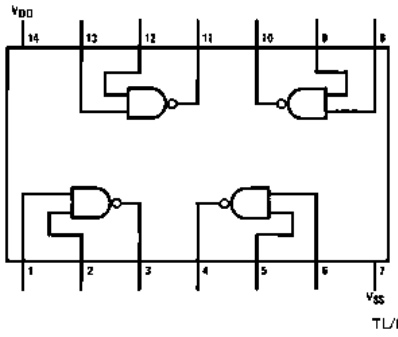
CD4001BC/CD4001BM
Dual-In-Line Package



TL/F/5939–3

Top View

CD4011BC/CD4011BM
Dual-In-Line Package



TL/F/5939–4

Top View

Order Number CD4001B or CD4011B

DC Electrical Characteristics CD4001BC, CD4011BC (Note 2)

Symbol	Parameter	Conditions	−40°C		+25°C			+85°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	V_{DD} = 5V, V_{IN} = V_{DD} or V_{SS}		1		0.004	1		7.5	μA
		V_{DD} = 10V, V_{IN} = V_{DD} or V_{SS}		2		0.005	2		15	μA
		V_{DD} = 15V, V_{IN} = V_{DD} or V_{SS}		4		0.006	4		30	μA
V_{OL}	Low Level Output Voltage	V_{DD} = 5V, I_O < 1 μA		0.05		0	0.05		0.05	V
		V_{DD} = 10V, I_O < 1 μA		0.05		0	0.05		0.05	V
		V_{DD} = 15V, I_O < 1 μA		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	V_{DD} = 5V, I_O < 1 μA	4.95		4.95	5		4.95		V
		V_{DD} = 10V, I_O < 1 μA	9.95		9.95	10		9.95		V
		V_{DD} = 15V, I_O < 1 μA	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	V_{DD} = 5V, V_O = 4.5V		1.5		2	1.5		1.5	V
		V_{DD} = 10V, V_O = 9.0V		3.0		4	3.0		3.0	V
		V_{DD} = 15V, V_O = 13.5V		4.0		6	4.0		4.0	V
V_{IH}	High Level Input Voltage	V_{DD} = 5V, V_O = 0.5V	3.5		3.5	3		3.5		V
		V_{DD} = 10V, V_O = 1.0V	7.0		7.0	6		7.0		V
		V_{DD} = 15V, V_O = 1.5V	11.0		11.0	9		11.0		V
I_{OL}	Low Level Output Current (Note 3)	V_{DD} = 5V, V_O = 0.4V	0.52		0.44	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.3		1.1	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	3.6		3.0	8.8		2.4		mA
I_{OH}	High Level Output Current (Note 3)	V_{DD} = 5V, V_O = 4.6V	−0.52		−0.44	−0.88		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.3		−1.1	−2.25		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−3.6		−3.0	−8.8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.30		-10^{-5}	−0.30		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.30		10^{-5}	0.30		1.0	μA

AC Electrical Characteristics* CD4001BC, CD4001BM

T_A = 25°C, Input t_r; t_f = 20 ns. C_L = 50 pF, R_L = 200k. Typical temperature coefficient is 0.3%/°C.

Symbol	Parameter	Conditions	Typ	Max	Units
t_{PHL}	Propagation Delay Time, High-to-Low Level	V_{DD} = 5V	120	250	ns
		V_{DD} = 10V	50	100	ns
		V_{DD} = 15V	35	70	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level	V_{DD} = 5V	110	250	ns
		V_{DD} = 10V	50	100	ns
		V_{DD} = 15V	35	70	ns
t_{THL}, t_{TLH}	Transition Time	V_{DD} = 5V	90	200	ns
		V_{DD} = 10V	50	100	ns
		V_{DD} = 15V	40	80	ns
C_{IN}	Average Input Capacitance	Any Input	5	7.5	pF
C_{PD}	Power Dissipation Capacity	Any Gate	14		pF

*AC Parameters are guaranteed by DC correlated testing.

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: All voltages measured with respect to V_{SS} unless otherwise specified.

Note 3: I_{OL} and I_{OH} are tested one output at a time.

AC Electrical Characteristics* CD4011BC, CD4011BM

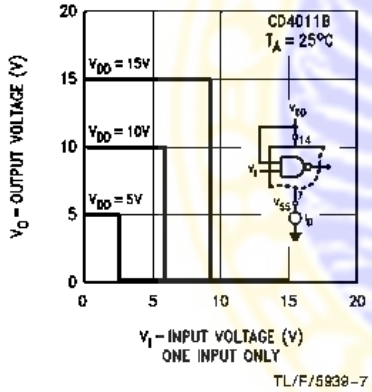
T_A = 25°C, Input t_r; t_f = 20 ns. C_L = 50 pF, R_L = 200k. Typical Temperature Coefficient is 0.3%/°C.

Symbol	Parameter	Conditions	Typ	Max	Units
t_{PHL}	Propagation Delay, High-to-Low Level	V_{DD} = 5V	120	250	ns
		V_{DD} = 10V	50	100	ns
		V_{DD} = 15V	35	70	ns
t_{PLH}	Propagation Delay, Low-to-High Level	V_{DD} = 5V	85	250	ns
		V_{DD} = 10V	40	100	ns
		V_{DD} = 15V	30	70	ns
t_{THL}, t_{TLH}	Transition Time	V_{DD} = 5V	90	200	ns
		V_{DD} = 10V	50	100	ns
		V_{DD} = 15V	40	80	ns
C_{IN}	Average Input Capacitance	Any Input	5	7.5	pF
C_{PD}	Power Dissipation Capacity	Any Gate	14		pF

*AC Parameters are guaranteed by DC correlated testing.

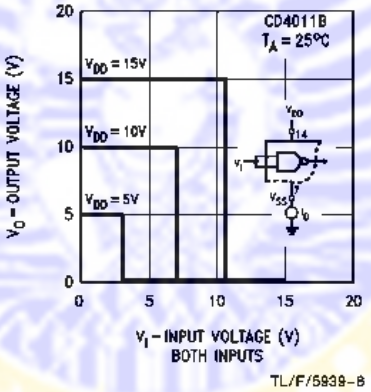
Typical Performance Characteristics

Typical Transfer Characteristics



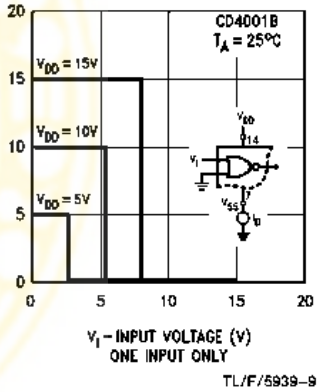
TL/F/5939–7

Typical Transfer Characteristics



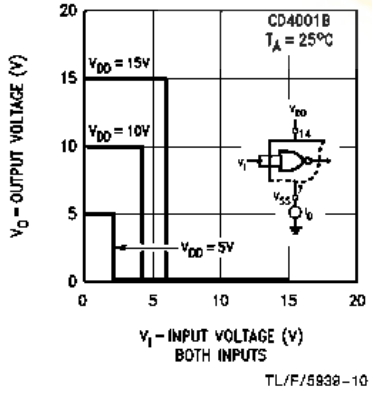
TL/F/5939–8

Typical Transfer Characteristics

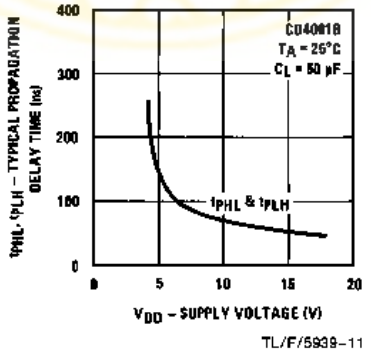


TL/F/5939–9

Typical Transfer Characteristics

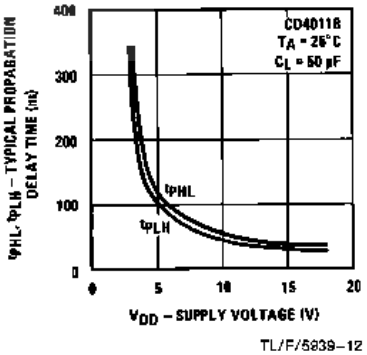


TL/F/5939–10



TL/F/5939–11

FIGURE 5



TL/F/5939–12

FIGURE 6

Typical Performance Characteristics (Continued)

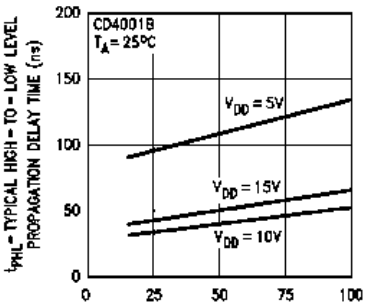


FIGURE 7

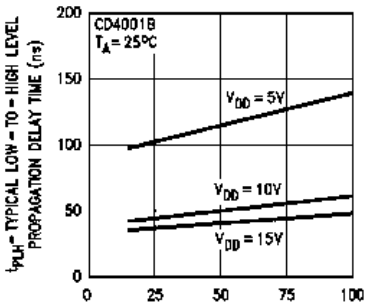


FIGURE 8

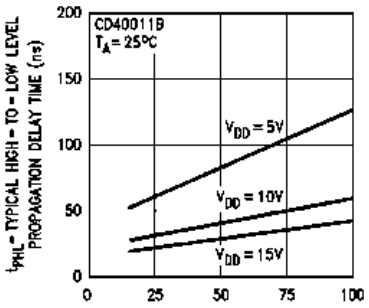


FIGURE 9

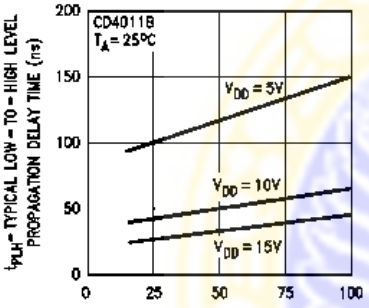


FIGURE 10

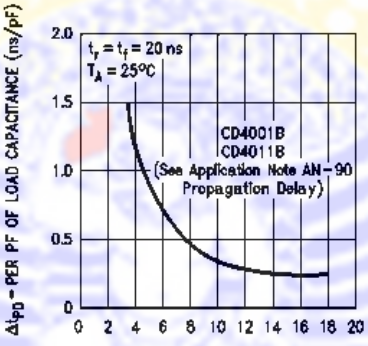


FIGURE 11

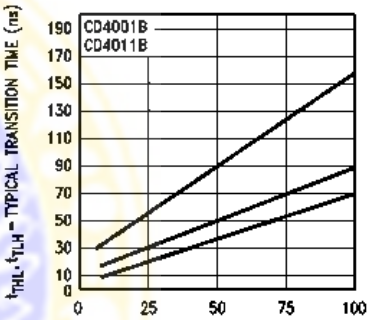


FIGURE 12

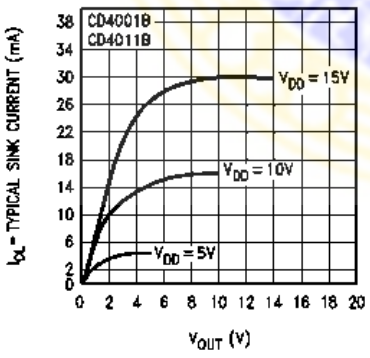


FIGURE 13

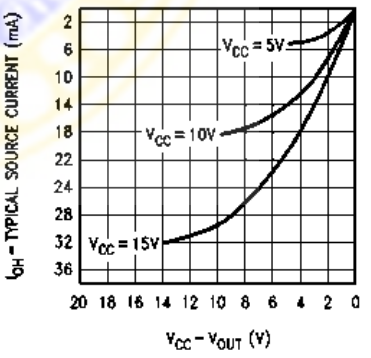


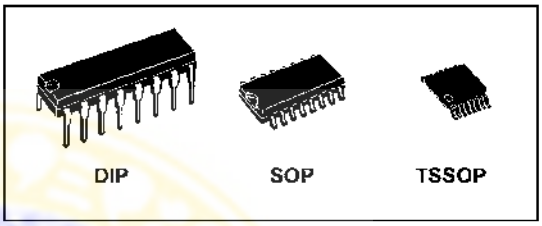
FIGURE 14

Lampiran 4 : *Datasheet* IC CD4051 BC

M74HC4051

SINGLE 8-CHANNEL ANALOG MULTIPLEXER/DEMULTIPLEXER

- LOW POWER DISSIPATION:
  I_{CC} = 4µA(MAX.) at T_A=25°C
- LOGIC LEVEL TRANSLATION TO ENABLE 5V LOGIC SIGNAL TO COMMUNICATE WITH ±5V ANALOG SIGNAL
- LOW "ON" RESISTANCE:
  70Ω TYP. (V_{CC} - V_{EE} = 4.5V)
  50Ω TYP. (V_{CC} - V_{EE} = 9V)
- WIDE ANALOG INPUT VOLTAGE RANGE:
  ±6V
- FAST SWITCHING:
  t_{pd} = 15ns (TYP.) at T_A = 25 °C
- LOW CROSSTALK BETWEEN SWITCHES
- HIGH ON/OFF OUTPUT VOLTAGE RATIO
- WIDE OPERATING SUPPLY VOLTAGE RANGE (V_{CC} - V_{EE}) = 2V TO 12V
- LOW SINE WAVE DISTORTION:
  0.02% at V_{CC} - V_{EE} = 9V
- HIGH NOISE IMMUNITY:
  V_{NIH} = V_{NIL} = 28 % V_{CC} (MIN.)
- PIN AND FUNCTION COMPATIBLE WITH 74 SERIES 4051



ORDER CODES

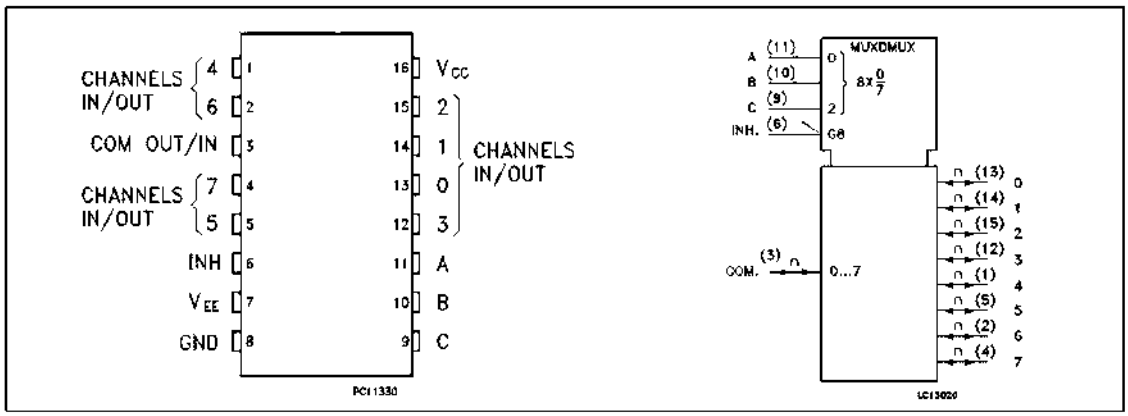
PACKAGE	TUBE	T & R
DIP	M74HC4051B1R	
SOP	M74HC4051M1R	M74HC4051RM13TR
TSSOP		M74HC4051TTR

DESCRIPTION

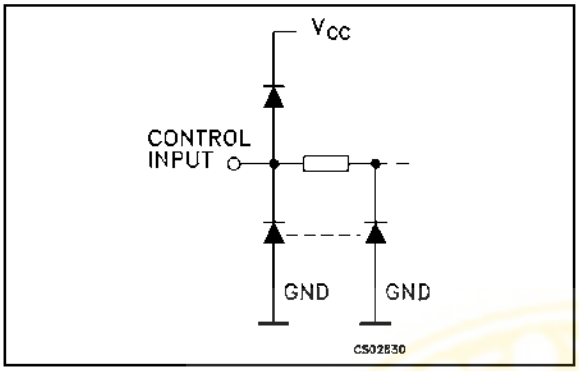
The M74HC4051 is a single eight-channel analog MULTIPLEXER/DEMULTIPLEXER fabricated with silicon gate C^2MOS technology and it is pin to pin compatible with the equivalent metal gate CMOS4000B series.

It contains 8 bidirectional and digitally controlled analog switches.
A built-in level shifting is included to allow an input range up to ±6V (peak) for an analog signal with digital control signal of 0 to 6V.
V_{EE} supply pin is provided for analog input signals. It has an inhibit (INH) input terminal to disable all the switches when is at high level. For operation as a digital multiplexer/demultiplexer, V_{EE} is connected to GND.
A, B and C control inputs select one channel out of eight.
All inputs are equipped with protection circuits against static discharge and transient excess voltage.

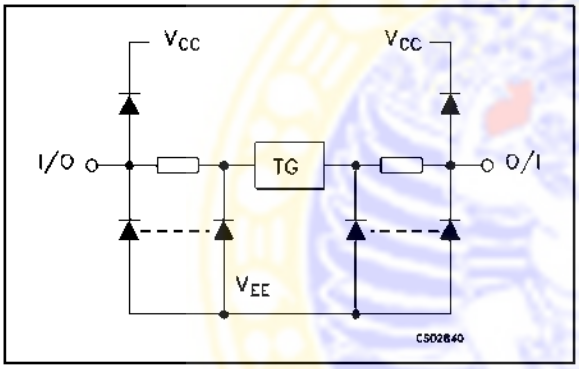
PIN CONNECTION AND IEC LOGIC SYMBOLS



CONTROL INPUT EQUIVALENT CIRCUIT



I/O EQUIVALENT CIRCUIT



PIN DESCRIPTION

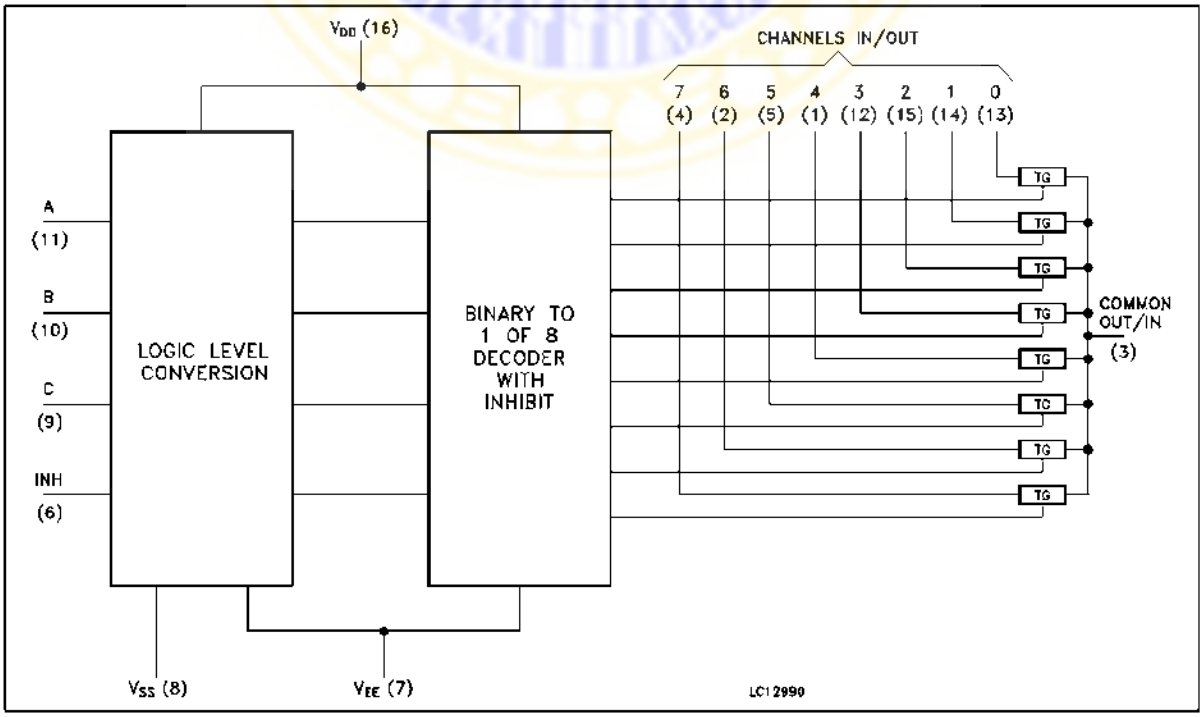
PIN No	SYMBOL	NAME AND FUNCTION
3	COM OUT/IN	Common Output/Input
6	INH	INHIBIT Input
7	V_{EE}	Negative Supply Voltage
11, 10, 9	A, B, C	Select Inputs
13, 14, 15, 12, 1, 5, 2, 4	0 to 7	Independent Input/Outputs
8	GND	Ground (0V)
16	V_{CC}	Positive Supply Voltage

TRUTH TABLE

INPUT STATE				ON CHANNEL
INH	C	B	A	
L	L	L	L	0
L	L	L	H	1
L	L	H	L	2
L	L	H	H	3
L	H	L	L	4
L	H	L	H	5
L	H	H	L	6
L	H	H	H	7
H	X	X	X	NONE

X: Don't care

FUNCTIONAL DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_{CC} - V_{EE}	Supply Voltage	-0.5 to +13	V
V_I	Control Input Voltage	-0.5 to V_{CC} + 0.5	V
$V_{I/O}$	Switch I/O Voltage	V_{EE} -0.5 to V_{CC} + 0.5	V
I_{CK}	Control Input Diode Current	± 20	mA
I_{IOK}	I/O Diode Current	± 20	mA
I_T	Switch Through Current	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500(*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied
(*) 500mW at 65 °C; derate to 300mW by 10mW/°C from 65°C to 85°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		2 to 6	V
V_{EE}	Supply Voltage		-6 to 0	V
V_{CC} - V_{EE}	Supply Voltage		2 to 12	V
V_I	Input Voltage		0 to V_{CC}	V
$V_{I/O}$	I/O Voltage		V_{EE} to V_{CC}	V
T_{op}	Operating Temperature		-55 to 125	°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2.0V	0 to 1000	ns
		V_{CC} = 4.5V	0 to 500	
		V_{CC} = 6.0V	0 to 400	

DC SPECIFICATIONS

Symbol	Parameter	Test Condition			Value							Unit
		V_{CC} (V)	V_{EE} (V)		T_A = 25°C			-40 to 85°C		-55 to 125°C		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IHC}	High Level Input Voltage	2.0			1.5			1.5		1.5		V
		4.5			3.15			3.15		3.15		
		6.0			4.2			4.2		4.2		
V_{ILC}	Low Level Input Voltage	2.0					0.5		0.5		0.5	V
		4.5					1.35		1.35		1.35	
		6.0					1.8		1.8		1.8	
R_{ON}	ON Resistance	4.5	GND	$V_I = V_{IHC}$ or V_{ILC} $V_{I/O} = V_{CC}$ to V_{EE} $I_{I/O} \leq 2mA$		85	180		225		270	Ω
		4.5	-4.5			55	120		150		180	
		6.0	-6.0			50	100		125		150	
		2.0	GND	$V_I = V_{IHC}$ or V_{ILC} $V_{I/O} = V_{CC}$ or V_{EE} $I_{I/O} \leq 2mA$		150						
		4.5	GND			70	150		190		230	
		4.5	-4.5			50	100		125		150	
		6.0	-6.0			45	80		100		120	
ΔR_{ON}	Difference of ON Resistance between switches	4.5	GND	$V_I = V_{IHC}$ or V_{ILC} $V_{I/O} = V_{CC}$ or V_{EE} $I_{I/O} \leq 2mA$		10	30		35		45	Ω
		4.5	-4.5			5	12		15		18	
		6.0	-6.0			5	10		12		15	
I_{OFF}	Input/Output Leakage Current (SWITCH OFF)	6.0	GND	$V_{OS} = V_{CC}$ or GND $V_{IS} = GND$ or V_{CC} $V_I = V_{ILC}$ or V_{IHC}			±0.06		± 0.6		± 1.2	µA
		6.0	-6.0				± 0.1		± 1		± 2	
I_{IZ}	Switch Input Leakage Current (SWITCH ON, OUTPUT OPEN)	6.0	GND	$V_{OS} = V_{CC}$ or GND $V_I = V_{IHC}$ or V_{ILC}			±0.06		± 0.6		± 1.2	µA
		6.0	-6.0				± 0.1		± 1		± 2	
I_I	Input Leakage Current	6.0	GND	$V_I = V_{CC}$ or GND			± 0.1		± 0.1		± 1	µA
I_{CC}	Quiescent Supply Current	6.0	GND	$V_I = V_{CC}$ or GND			4		40		80	µA
		6.0	-6.0				8		80		160	

Lampiran 5 : *Datasheet* Transistor C945

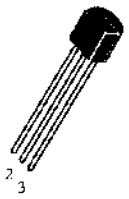
WEITRON

C945

NPN Transistors

Pb **Lead(Pb)-Free**

TO-92



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	50	Vdc
Collector-Base Voltage	V_{CBO}	60	Vdc
Emitter-Base Voltage	V_{EBO}	5.0	Vdc
Collector Current-Continuous	I_C	150	mAdc
Total Device Dissipation TA=25°C	P_D	0.4	W
Junction Temperature	T_J	+150	°C
Storage Temperature	T_{STG}	-40 to + 150	°C

ELECTRICAL CHARACTERISTICS

Characteristics	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Breakdown Voltage (I_C=100 uAdc, I_B=0)	$V_{(BR)CEO}$	50	-	Vdc
Collector-Base Breakdown Voltage (I_C= 1 mAdc, I_E=0)	$V_{(BR)CBO}$	60	-	Vdc
Emitter-Base Breakdown Voltage (I_E=100 uAdc, I_C=0)	$V_{(BR)EBO}$	5.0	-	Vdc
Collector Cutoff Current (V_{CE}=60 Vdc, I_E= 0)	I_{CEO}	-	0.1	uAdc
Collector Cutoff Current (V_{CB}= 45 Vdc, I_E=0)	I_{CBO}	-	0.1	uAdc
Emitter Cutoff Current (V_{EB}= 5.0 Vdc, I_C=0)	I_{EBO}	-	0.1	uAdc

C945

WEITRON

ELECTRICAL CHARACTERISTICS (T_A=25 °C unless otherwise noted) (Countinued)

Characteristics	Symbol	Min	Typ	Max	Unit
ON CHARACTERISTICS					
DC Current Gain V_{CE}=6.0V, I_C=1mA V_{CE}=6.0V, I_C=0.1mA	h_{FE1} h_{FE2}	70 40	-	700	-
Collector-Emitter Saturation Voltage I_C=100mA, I_B=10mA	$V_{CE(sat)}$	-	-	0.3	V
Base-Emitter Voltage I_C=100mA, I_B=10mA	$V_{BE(sat)}$	-	-	1.0	V
TransitionFrequence V_{CE} = 6V, I_C = 10mA, f = 30MHz	f-	200	-	-	MHz
Collector Output Capacitance V_{CB} = 10V, I_E = 0, f = 1MHz	Cob	-	-	3.0	pF
Noise figure V_{CE} = 6V, I_C = 0.1mA, Rg = 10kΩ, f = 1KMHz	NF	-	4.0	10	dB

CLASSIFICATION OF h_{FE1}

Rank	O	Y	GR	BL
Range	70-140	120-240	200-400	350-700

C945

WEITRON

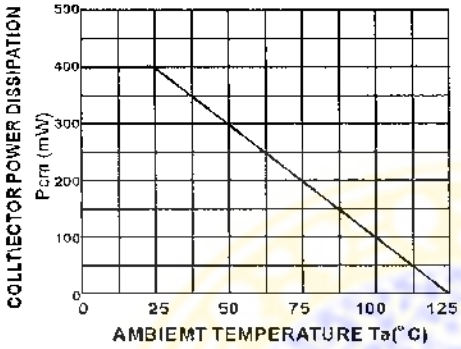


FIG1. Total Power Dissipation vs Ambient Temperature

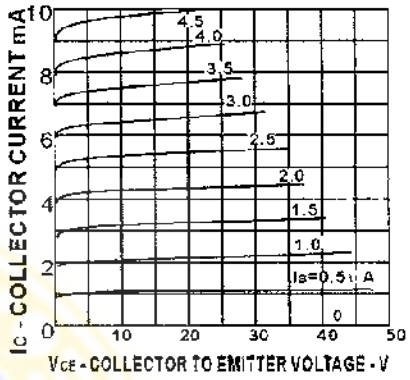


FIG.2 Collector Current vs Collector to Emitter Voltage

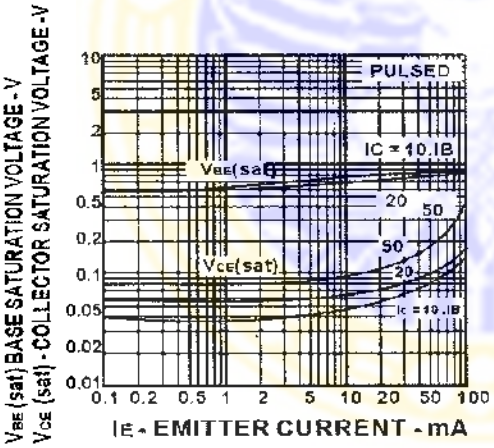


FIG.3 Collector and Bade Saturation Voltage vs Collector Current

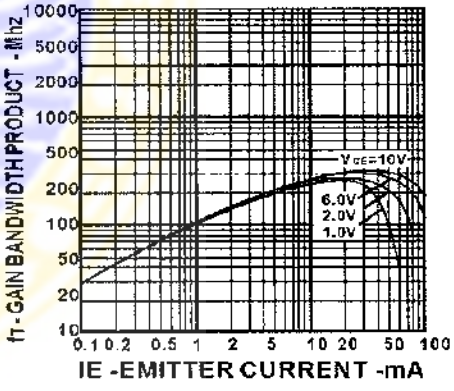


FIG.4 Gain Bandwidth Product vs Emitter Current

Lampiran 6 : *Datasheet* Transistor C2073

FAIRCHILD
SEMICONDUCTOR™

KSC2073

TV Vertical Deflection Output

- Complement to KSA940
- Collector-Base Voltage : V_{CBO} = 150V

TO-220

1.Base 2.Collector 3.Emitter

NPN Epitaxial Silicon Transistor

Absolute Maximum Ratings T_C=25°C unless otherwise noted

Symbol	Parameter	Value	Units
V_{CBO}	Collector-Base Voltage	150	V
V_{CEO}	Collector-Emitter Voltage	150	V
V_{EBO}	Emitter-Base Voltage	5	V
I_C	Collector Current	1.5	A
P_C	Collector Dissipation (T_C=25°C)	25	W
T_J	Junction Temperature	150	°C
T_{STG}	Storage Temperature	- 55 ~ 150	°C

Electrical Characteristics T_C=25°C unless otherwise noted

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
BV_{CBO}	Collector-Base Breakdown Voltage	I_C = 500μA, I_E = 0	150			V
BV_{CEO}	Collector-Emitter Breakdown Voltage	I_C = 10mA, I_B = 0	150			V
BV_{EBO}	Emitter-Base Breakdown Voltage	I_E = - 500μA, I_C = 0	5			V
I_{CBO}	Collector Cut-off Current	V_{CB} = 120V, I_E = 0			10	μA
h_{FE}	DC Current Gain	V_{CE} = 10V, I_C = 0.5A	40	75	140	
V_{CE}(sat)	Collector-Emitter Saturation Voltage	I_C = 500mA, I_B = 50mA			1	V
f_T	Current Gain Bandwidth Product	V_{CE} = 10V, I_C = 0.5A		4		MHz
C_{ob}	Output Capacitance	V_{CB} =10V, I_E = 0 f = 1MHz		50		pF

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Rev. A, February 2000

KSC2073

Typical Characteristics

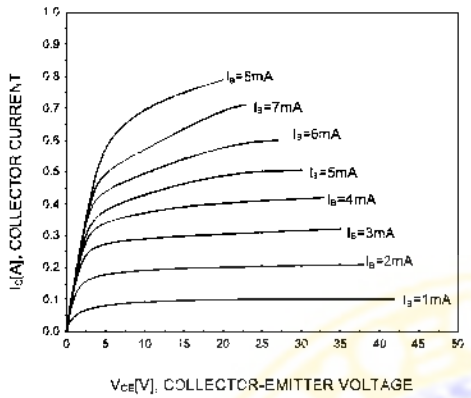

Figure 1. Static Characteristic

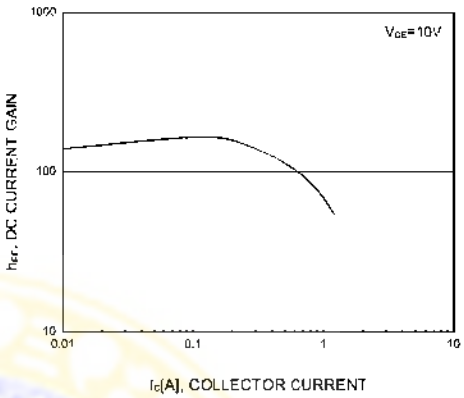

Figure 2. DC current Gain

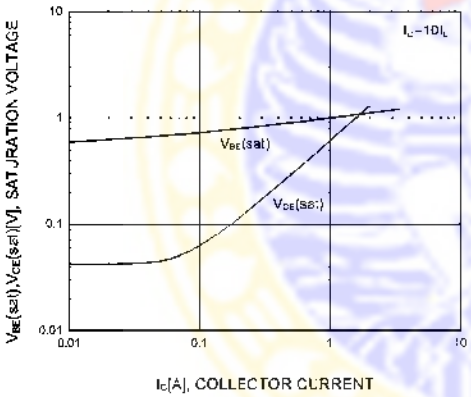

Figure 3. Base-Emitter Saturation Voltage Collector-Emitter Saturation Voltage

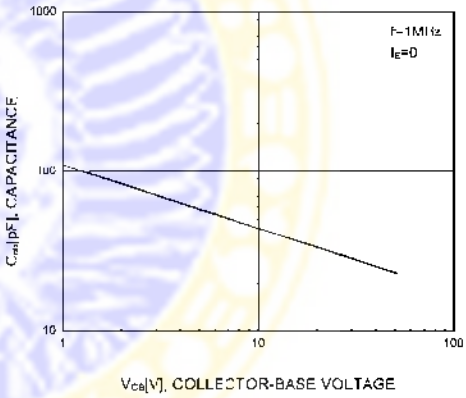

Figure 4. Collector-Emitter On Voltage

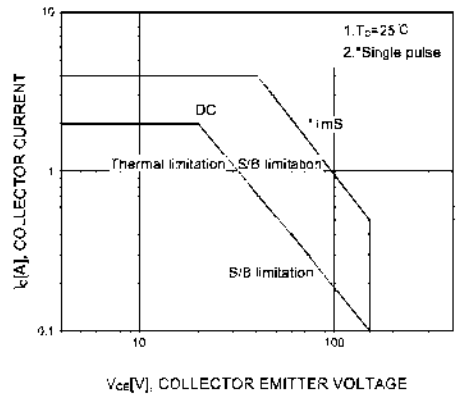

Figure 5. Safe Operating Area

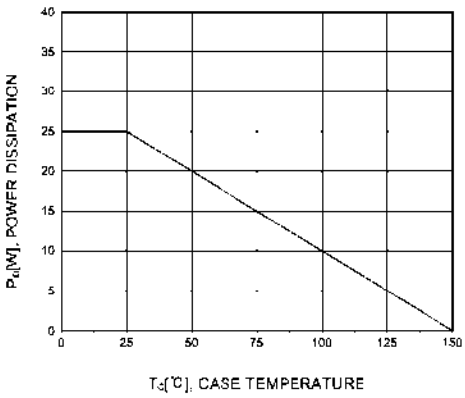

Figure 6. Power Derating

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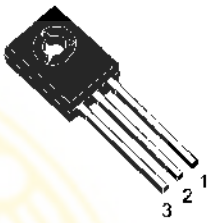
Lampiran 7 : *Datasheet* Transistor BD139

BD135
BD139

NPN SILICON TRANSISTORS

Type	Marking
BD135	BD135
BD135-10	BD135-10
BD135-16	BD135-16
BD139	BD139
BD139-10	BD139-10
BD139-16	BD139-16



SOT-32

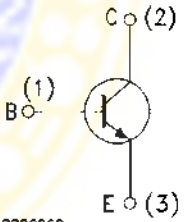
- STMicroelectronics PREFERRED SALESTYPES

DESCRIPTION

The BD135 and BD139 are silicon Epitaxial Planar NPN transistors mounted in Jedec SOT-32 plastic package, designed for audio amplifiers and drivers utilizing complementary or quasi-complementary circuits.

The complementary PNP types are BD136 and BD140 respectively.

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value		Unit
		BD135	BD139	
V_{CBO}	Collector-Base Voltage (I_E = 0)	45	80	V
V_{CEO}	Collector-Emitter Voltage (I_B = 0)	45	80	V
V_{EBO}	Emitter-Base Voltage (I_C = 0)	5		V
I_C	Collector Current	1.5		A
I_{CM}	Collector Peak Current	3		A
I_B	Base Current	0.5		A
P_{tot}	Total Dissipation at $T_c \leq 25$ °C	12.5		W
P_{tot}	Total Dissipation at $T_{amb} \leq 25$ °C	1.25		W
T_{stg}	Storage Temperature	-65 to 150		°C
T_j	Max. Operating Junction Temperature	150		°C

BD135 / BD139

THERMAL DATA

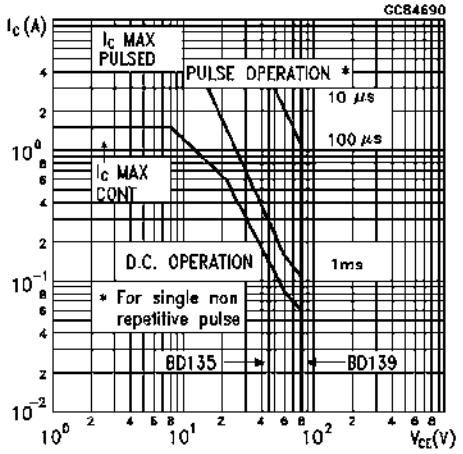
$R_{thj\text{-}case}$	Thermal Resistance Junction-case	Max	10	°C/W

ELECTRICAL CHARACTERISTICS (T_{case} = 25 °C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{CBO}	Collector Cut-off Current (I_E = 0)	V_{CB} = 30 V V_{CB} = 30 V T_C = 125 °C			0.1 10	µA µA
I_{EBO}	Emitter Cut-off Current (I_C = 0)	V_{EB} = 5 V			10	µA
$V_{CEO(sus)}$*	Collector-Emitter Sustaining Voltage (I_B = 0)	I_C = 30 mA for **BD135** for **BD139**	 45 80			 V V
$V_{CE(sat)}$*	Collector-Emitter Saturation Voltage	I_C = 0.5 A I_B = 0.05 A			0.5	V
V_{BE}*	Base-Emitter Voltage	I_C = 0.5 A V_{CE} = 2 V			1	V
h_{FE}*	DC Current Gain	I_C = 5 mA V_{CE} = 2 V I_C = 150 mA V_{CE} = 2 V I_C = 0.5 A V_{CE} = 2 V	25 40 25		 250	
h_{FE}	h_{FE} Groups	I_C = 150 mA V_{CE} = 2 V for **BD135/BD139** group-10 for **BD135/BD139** group-16	 63 100		 160 250	

* Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %

Safe Operating Area



Lampiran 8 : Perhitungan jarak antar pulsa atau periode total pada rangkaian Osilator.

$t_{LO} = 0{,}693\ R_B C$

$t_{HI} = 0{,}693(R_A + R_B)C$

Periode total (T) = $t_{H1} + t_{L0}$

$= 0{,}693(R_A + 2R_B)C$

Frekuensi Osilasi (f) = $\frac{1}{T}$

Duty Cycle (D) = $\frac{RB}{RA+2RB}$

$t_{L0} = 0{,}693 x R_B\, xC$

$= 0{,}693 x 1K\Omega x 10 F$

$= 0{,}693 x 1 x 10^3 \Omega x 10 x 10^{-6} F$

$= 0{,}00693\ s$

$t_{H1} = 0{,}693 x (R_A + R_B)\, xC$

$= 0{,}693 x (15K\Omega + 1K\Omega) x 10 F$

$= 0{,}693 x 16 x 10^3 \Omega x 10 x 10^{-6} F$

$= 0{,}11088\ s$

Periode Total (T) = $t_{L0} + t_{H1}$

$= 0{,}00693\ s + 0{,}11088\ s$

$= 0{,}11781\ s$

$= 117{,}81\ ms$

Frekuensi $= \frac{1}{T}$

$= \frac{1}{0{,}11781\ s}$

$= \mathbf{8{,}488\ Hz}$

Periode Total (T) = Jarak Antar Pulsa = 117,81 *ms*

Lampiran 9 : Perhitungan ADC (*Analog to Digital Converter*) untuk mendeteksi respon refleks pada sensor *knee joint*.

a. Perhitungan Tegangan per perubahan derajat potensiometer ($V°$)

$$V° = \frac{Vref}{\Delta\theta}$$

$$V° = \frac{5V}{140° - 90°}$$

$$V° = \frac{5V}{50°}$$

$$V° = 0{,}1V$$

Jadi tegangan per perubahan derajat potensiometer ($V°$) $= 0{,}1V$

b. Perhitungan quantisasi ADC

$$Quantisasi\ ADC = \frac{Vref}{Level\ resolusi\ ADC}$$

$$Quantisasi\ ADC = \frac{5V}{256}$$

$$Quantisasi\ ADC = 0{,}01953\ V$$

Jadi quantisasi ADC adalah sebesar 0,01953V

c. Perhitungan untuk mencari faktor pengali 'A'

$$V° = Quantisasi\ ADCxA$$

$$A = \frac{V°}{Quantisasi\ \ ADC}$$

$$A = \frac{0{,}1}{0{,}01953}$$

$$A = 5{,}12033$$

d. Perhitungan besar sudut untuk desain sensor *knee joint*

$$Sudut\ knee\ joint = \ V° = Quantisasi\ ADCxA$$

$$Sudut\ knee\ Joint = V° = 0{,}01953x5{,}12033$$

Lampiran 10 : *Listing* program yang terdapat pada alat *electrical stimulator.*

```
/*****************************************************
This program was produced by the
CodeWizardAVR V2.03.4 Standard
Automatic Program Generator
© Copyright 1998-2008 Pavel Haiduc, HP InfoTech s.r.l.
http://www.hpinfotech.com
Project :
Version :
Date    : 24/06/2012
Author  :
Company :
Comments:
Chip type           : ATmega8535
Program type        : Application
Clock frequency     : 11,059200 MHz
Memory model        : Small
External RAM size   : 0
Data Stack size     : 128
*****************************************************/
#include <mega8535.h>
#include <lcd.h>
#include <delay.h>
#include <stdio.h>
#include <stdlib.h>
#define ADC_VREF_TYPE 0x20
unsigned char read_adc(unsigned char adc_input)
{ADMUX=adc_input | (ADC_VREF_TYPE & 0xff);
delay_us(10); ADCSRA|=0x40; while ((ADCSRA & 0x10)==0);
ADCSRA|=0x10; return ADCH;}
#asm
   .equ __lcd_port=0x15 ;PORTC
#endasm
#include <lcd.h>
unsigned char dtkey,dt; unsigned char buffer[16]; //Untuk buffer sprintf
void detek_key (void); unsigned int vsdt,as; float sudut, data1, data2, data3;
void detek_key (void)
{PORTB.4=0; dt = (~PINB & 0x0F);
switch (dt)
{case 1 :{dtkey = 1; PORTD.0=0; PORTD.1=0; PORTD.2=0;break;}
case 2:{ dtkey = 2; PORTD.0=0; PORTD.1=0; PORTD.2=1; break;}
 case 4:{dtkey = 3; PORTD.0=0; PORTD.1=1; PORTD.2=0; break;}
case 8:dtkey = 10 ;break; }; PORTB.4 = 1 ; PORTB.5 = 0;
dt = (~PINB & 0x0F); switch (dt)
{case 1 : { dtkey = 4; PORTD.0=0;  PORTD.1=1;  PORTD.2=1; break;}
```

```
case 2 :{dtkey = 5;  PORTD.0=1;   PORTD.1=0;  PORTD.2=0; break;}
case 4 :{dtkey = 6;  PORTD.0=1;  PORTD.1=0;  PORTD.2=1; break;}
case 8 : dtkey = 11; break;}; PORTB.5 = 1 ; PORTB.6 = 0;
dt = (~PINB & 0x0F); switch (dt)
{case 1: {dtkey = 7;  PORTD.0=1;   PORTD.1=1;   PORTD.2=0; break;}
case 2:{dtkey = 8;  PORTD.0=1;  PORTD.1=1;  PORTD.2=1; break;}
case 4 : dtkey = 9 ; break;
case 8 : dtkey = 12 ; break;};
PORTB.6 = 1 ; PORTB.7 = 0; dt = (~PINB & 0x0F);
switch (dt){case 1:dtkey = 14; break; case 2:dtkey = 0; break; case 4:dtkey = 15;
            break; case 8:dtkey = 13;break;};
PORTB.7 = 1;}
void main(void) PORTA=0x00; DDRA=0x00; PORTB=0xFF; DDRB=0xF0;
PORTC=0x00; DDRC=0x00; PORTD=0x00; DDRD=0x0F; ACSR=0x80;
SFIOR=0x00; ADMUX=ADC_VREF_TYPE & 0xff; ADCSRA=0x86;
SFIOR&=0xEF; as=0;
lcd_init(16); lcd_gotoxy(0,0); lcd_putsf("PUTRI NI'MATUL L");
lcd_gotoxy(0,1); lcd_putsf("=NIM:080810047="); delay_ms(4000);
lcd_clear(); lcd_gotoxy(0,0); lcd_putsf("=DESAIN-ES-4-HR=");
lcd_gotoxy(0,1); lcd_putsf("=TKNOBIOMDK-FST="); delay_ms(3000);
lcd_clear(); lcd_gotoxy(0,0); lcd_putsf("TEKAN HURUF A"); lcd_gotoxy(0,1);
lcd_putsf("UNTUK START ES"); delay_ms(3000); lcd_clear(); lcd_gotoxy(0,0);
lcd_putsf("TEKAN ANGKA 1-8"); lcd_gotoxy(0,1);
lcd_putsf("U/ ATUR STIMULUS"); delay_ms(3000); lcd_clear();
while (1)
  {vsdt=read_adc(0); sudut=(vsdt*(0.01953*5.12033)); data1=sudut;
   detek_key(); lcd_gotoxy(0,1);  sprintf(buffer,"%d",dtkey);  lcd_puts(buffer);
   delay_ms(1000); if(dtkey == 9)
{as++;}
if(as!=0)
{vsdt=read_adc(0); sudut=(vsdt*(0.01953*5.12033)); data2=sudut; PORTD.3=0;
  data3=data2-data1;  if(data3>0)
 {PORTD.3=1; #asm rjmp 0x00;_reset  #endasm}
  if(data3<0) {vsdt=read_adc(0); sudut=(vsdt*(0.01953*5.12033));
              data2=sudut;    PORTD.3=0; data3=data2-data1;}}}};
```

Lampiran 11 : Perhitungan pada pengujian Rangkaian Osilator dan penguat Tegangan

a. Perhitungan tegangan stimulasi puncak (Vp)

$$Vp = Tinggi\ vertikal\ gelombang x probe x skala\ v/div$$
$$Vp = 7{,}1 div x 10 x 5 v/div$$
$$Vp = 355 Volt$$

b. Perhitungan dalam menentukan *duty cycle*

$$Lebar\ pulsa\ on = horizontal\ gelombang x skala\ time/div$$

$$Lebar\ pulsa\ on = 0{,}1\ div\ x 0{,}2 m time/div$$
$$Lebar\ pulsa\ on = 0{,}02 \text{ms}$$
$$Lebar\ pulsa\ on = 20 s$$
$$duty\ cycle = \frac{Lebar\ Pulsa\ on}{Lebar\ Pulsa\ off}$$
$$duty\ cycle = \frac{20 s}{117{,}81 ms}$$
$$duty\ cycle = \frac{20 x 10^{-6}}{117{,}81 x 10^{-3}}$$
$$duty\ cycle = 0{,}1697 x 10^{-3}$$
$$Persentase\ duty\ cycle = 0{,}01697\%$$

Lampiran 12 : Perhitungan pada pengujian Rangkaian *Output* Level Tegangan Stimulasi (Vp)

a. Perhitungan tegangan keluaran secara manual:

$Rtot = R1 + R2 + R3 + R4 + R5 + R6 + R7 + R8$

$Rtot = 4{,}71K\Omega + 4{,}7K\Omega + 3{,}3K\Omega + 1{,}56K\Omega + 1{,}49K\Omega + 1{,}2K\Omega + 1{,}53K + 1{,}2K\Omega$

$Rtot = 19{,}69\ K\Omega$

$VO_1 = \frac{R1}{Rtot} xVOmaks$

$VO_1 = \frac{4{,}71K\Omega}{19{,}69K\Omega} x355V$

$\boldsymbol{VO_1 = 84,918V}$

$VO_2 = \frac{R1+R2}{Rtot} xVOmaks$

$VO_2 = \frac{4{,}71K\Omega+4{,}7K\Omega}{19{,}69K\Omega} x355V$

$\boldsymbol{VO_2 = 169,657V}$

$VO_3 = \frac{R1+R2+R3}{Rtot} xVOmaks$

$VO_3 = \frac{4{,}71K\Omega+4{,}7K\Omega+3{,}3K\Omega}{19{,}69K\Omega} x355V$

$\boldsymbol{VO_3 = 229,154V}$

$VO_4 = \frac{R1+R2+R3+R4}{Rtot} xVOmaks$

$VO_4 = \frac{4{,}71K\Omega+4{,}7K\Omega+3{,}3K\Omega+1{,}56K\Omega}{19{,}69K\Omega} x355V$

$\boldsymbol{VO_4 = 257,28V}$

$VO_5 = \frac{R1+R2+R3+R4+R5}{Rtot} xVOmaks$

$VO_5 = \frac{4{,}71+4{,}7+3{,}3K\Omega+1{,}56K\Omega+1{,}49K\Omega}{19{,}69K\Omega} x355V$

$\boldsymbol{VO_5 = 284,144V}$

$VO_6 = \frac{R1+R2+R3+R4+R5+R6}{Rtot} xVOmaks$

$VO_6 = \frac{4{,}71+4{,}7+3{,}3+1{,}56+1{,}49+1{,}2}{19{,}69K\Omega} x355V$

$\boldsymbol{VO_6 = 305,779V}$

$VO_7 = \frac{1+R2+R3+R4+R5+R6+R7}{Rtot} xVOmaks$

$VO_7 = \frac{4{,}71+4{,}7+3{,}3+1{,}56+1{,}49+1{,}2+1{,}53+1{,}2}{19{,}69K\Omega} x355V$

$\boldsymbol{VO_7 = 333,364V}$

$VO_8 = \frac{Rtot}{Rtot} xVOmaks$

$VO_8 = \frac{19{,}69K\Omega}{19{,}69K\Omega} x355V$

$\boldsymbol{VO_8 = 355V}$

b. Perhitungan tingkat kestabilan pada kedelapan keluaran level tegangan stimulasi (Vp) tanpa beban.

Kesalahan $Akurasi\ Tegangan = \frac{Nilai\ Standar\ Deviasi}{Rata - rata} x100\%$

Kesalahan $Akurasi\ Tegangan = \frac{1{,}054}{225{,}5} x100\%$

Kesalahan $Akurasi\ Tegangan = 0{,}467\%$

Tingkat Kestabilan $= 100\% -$ Kesalahan $Akurasi\ Tegangan$

$= 100\% - 0{,}467\%$

$= 99{,}533\%$

Lampiran 13 : Pembuktian perhitungan arus yang dialirkan oleh *electrical stimulator* yang dirancang

a. Perhitungan Vrms pada kondisi tanpa beban untuk setiap tegangan stimulasi (Vp) pada kondisi tanpa beban.

$Periode\ Total\ (T) = Jarak\ Antar\ Pulsa = 20\ \mu s$

$Lebar\ pulsa = 20\ \mu s$

$duty\ cycle = 0{,}1697x10^{-3}\ s$

$$Vrms = \frac{1}{T}\left(\frac{1}{2}.Vp.Lebar\ pulsa\right)$$

$$Vrms = \frac{1}{2}.Vp.\left(\frac{Lebar\ pulsa}{T}\right)$$

$$Vrms = \frac{1}{2}.Vp.\left(\frac{Lebar\ pulsa}{Jarak\ Antar\ Pulsa}\right)$$

$$Vrms = \frac{1}{2}.Vp.duty\ cycle$$

- $Vrms1 = \frac{1}{2}.Vp1.duty\ cycle$

  $Vrms1 = \frac{1}{2}x85x0{,}1697x10^{-3}\ s$

  $\boldsymbol{Vrms1 = 7{,}21225\ mV}$

- $Vrms2 = \frac{1}{2}.Vp2.duty\ cycle$

  $Vrms2 = \frac{1}{2}x170x0{,}1697x10^{-3}\ s$

  $\boldsymbol{Vrms2 = 14{,}42450\ mV}$

- $Vrms3 = \frac{1}{2}.Vp3.duty\ cycle$

  $Vrms3 = \frac{1}{2}x225x0{,}1697x10^{-3}\ s$

  $\boldsymbol{Vrms3 = 19{,}09125\ mV}$

- $Vrms6 = \frac{1}{2}.Vp6.duty\ cycle$

  $Vrms6 = \frac{1}{2}x305x0{,}1697x10^{-3}\ s$

  $\boldsymbol{Vrms6 = 25{,}87925\ mV}$

- $Vrms4 = \frac{1}{2}.Vp4.duty\ cycle$

  $Vrms4 = \frac{1}{2}x255x0{,}1697x10^{-3}\ s$

  $\boldsymbol{Vrms4 = 21{,}63675\ mV}$

- $Vrms7 = \frac{1}{2}.Vp7.duty\ cycle$

  $Vrms7 = \frac{1}{2}x335x0{,}1697x10^{-3}\ s$

  $\boldsymbol{Vrms7 = 28{,}42475\ mV}$

- $Vrms5 = \frac{1}{2}.Vp5.duty\ cycle$

  $Vrms5 = \frac{1}{2}x285x0{,}1697x10^{-3}\ s$

  $\boldsymbol{Vrms5 = 24{,}18225\ mV}$

- $Vrms8 = \frac{1}{2}.Vp8.duty\ cycle$

  $Vrms8 = \frac{1}{2}x355x0{,}1697x10^{-3}\ s$

  $\boldsymbol{Vrms8 = 30{,}12175\ mV}$

b. Perhitungan Vrms pada kondisi terhubung beban untuk setiap tegangan stimulasi (Vp) pada kondisi terhubung beban.

$Periode\ Total\ (T) = Jarak\ Antar\ Pulsa = 20\ \mu s$

$Lebar\ pulsa = 20\ \mu s$

$duty\ cycle = 0{,}1697x10^{-3}\ s$

$$Vrms = \frac{1}{T}\left(\frac{1}{2}.Vp.Lebar\ pulsa\right)$$

$$Vrms = \frac{1}{2}.Vp.duty\ cycle$$

$$Vrms = \frac{1}{2}.Vp.\left(\frac{Lebar\ pulsa}{T}\right)$$

$$Vrms\frac{1}{2}.Vp.\left(\frac{Lebar\ pulsa}{Jarak\ Antar\ Pulsa}\right)$$

- $Vrms1a = \frac{1}{2}.Vp1.duty\ cycle$

  $Vrms1a = \frac{1}{2}x70x0{,}1697x10^{-3}\ s$

  $\boldsymbol{Vrms1a = 5{,}93950\ mV}$
- $Vrms2a = \frac{1}{2}.Vp2.duty\ cycle$

  $Vrms2a = \frac{1}{2}x115x0{,}1697x10^{-3}\ s$

  $\boldsymbol{Vrms2a = 9{,}75775\ mV}$
- $Vrms3a = \frac{1}{2}.Vp3.duty\ cycle$

  $Vrms3a = \frac{1}{2}x155x0{,}1697x10^{-3}\ s$

  $\boldsymbol{Vrms3a = 13{,}15175\ mV}$
- $Vrms4a = \frac{1}{2}.Vp4.duty\ cycle$

  $Vrms4a = \frac{1}{2}x180x0{,}1697x10^{-3}\ s$

  $\boldsymbol{Vrms4a = 15{,}27300\ mV}$
- $Vrms5a = \frac{1}{2}.Vp5.duty\ cycle$
- $Vrms5a = \frac{1}{2}x200x0{,}1697x10^{-3}\ s$

  $\boldsymbol{Vrms5a = 16{,}97000\ mV}$
- $Vrms6a = \frac{1}{2}.Vp6.duty\ cycle$

  $Vrms6a = \frac{1}{2}x220x0{,}1697x10^{-3}\ s$

  $\boldsymbol{Vrms6a = 18{,}66700\ mV}$
- $Vrms7a = \frac{1}{2}.Vp7.duty\ cycle$

  $Vrms7a = \frac{1}{2}x240x0{,}1697x10^{-3}\ s$

  $\boldsymbol{Vrms7a = 20{,}36400\ mV}$
- $Vrms8a = \frac{1}{2}.Vp8.duty\ cycle$

  $Vrms8a = \frac{1}{2}x260x0{,}1697x10^{-3}\ s$

  $\boldsymbol{Vrms8a = 22{,}06100\ mV}$

c. Perhitungan Irms pada kondisi terhubung beban untuk setiap tegangan stimulasi (Vp) pada kondisi terhubung beban.

$Resistansi\ Tendon = 138K\Omega$

$i_{rms} = \frac{Vrms}{Resistansi\ \ Tendon}$

- $i_{rms1} = \frac{Vrms\ 1a}{Resistansi\ \ Tendon}$

  $i_{rms1} = \frac{5{,}93950\ mV}{138K\Omega}$

  $i_{rms1} = 0{,}04304\ \square A$
- $i_{rms2} = \frac{Vrms\ 2a}{Resistansi\ \ Tendon}$

  $i_{rms2} = \frac{9{,}7577\ \text{mV}}{138K\Omega}$

  $i_{rms2} = 0{,}07071\ \square A$
- $i_{rms3} = \frac{Vrms\ 3a}{Resistansi\ \ Tendon}$

  $i_{rms3} = \frac{13{,}15175\ \text{mV}}{138K\Omega}$

  $i_{rms3} = 0{,}09530\ \square A$
- $i_{rms4} = \frac{Vrms\ 4a}{Resistansi\ \ Tendon}$

  $i_{rms4} = \frac{15{,}27300\ \text{mV}}{138K\Omega}$

  $i_{rms4} = 0{,}11067\ \square A$
- $i_{rms5} = \frac{Vrms\ 5a}{Resistansi\ \ Tendon}$

  $i_{rms5} = \frac{16{,}97000\ \text{mV}}{138K\Omega}$

  $i_{rms5} = 0{,}12297\ \square A$
- $i_{rms6} = \frac{Vrms\ 6a}{Resistansi\ \ Tendon}$

  $i_{rms6} = \frac{18{,}66700\ \text{mV}}{138K\Omega}$

  $i_{rms6} = 0{,}13527\ \square A$
- $i_{rms7} = \frac{Vrms\ 7a}{Resistansi\ \ Tendon}$

  $i_{rms7} = \frac{20{,}36400\ \text{mV}}{138K\Omega}$

  $i_{rms7} = 0{,}14756\ \square A$
- $i_{rms8} = \frac{Vrms\ 8a}{Resistansi\ \ Tendon}$

  $i_{rms8} = \frac{22{,}06100\ \text{mV}}{138K\Omega}$

  $i_{rms8} = 0{,}15986\ \square A$